A/D CONVERSION WITH FUZZY MEMBERSHIP FUNCTION

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ABSTRACT

This paper presents a general architecture of an A/D converter whose input-output transfer characteristic has the shape of a typical fuzzy membership function. Indeed, the proposed A/D converter performs a fuzzification operation from input to output through a programmable trapezoidal function. The proposed architecture requires a conventional A/D converter, a comparator, some inverters and switches, thus allowing to save silicon area while maintaining good flexibility and programmability. Moreover, it does not depend on the converter architecture and can be applied to every A/D converter.

1 INTRODUCTION

Fuzzy inference was developed to handle imprecise knowledge using common sense rule, like human reasoning [1–3]. Started in late 70s, fuzzy logic controllers are becoming a practical reality, with more and more applications in consumer electronics. Research is devoted to implement fuzzy logic using both digital and analog hardware [4–16], to realise fast and efficient systems for real-time application.

Membership function is a key element in a fuzzy controller. Also called "fuzzification", it is a non-linear function that measures the compatibility of an object with the concept represented by a fuzzy set [3]. When the input of a fuzzy controller is an analog signal and processing is in digital domain, an A/D converter is required at the input front-end. Then the fuzzification can be obtained through a look-up table or with suitable digital circuitry. In both cases the required silicon area is not negligible even for low-resolution signals.

This communication presents a novel approach to achieve the fuzzification of input signals (i. e., their membership function). The basic idea is to combine A/D conversion and membership function into a single functional block. The proposed solution allows us to save a significant amount of silicon area, while maintaining good flexibility and programmability. Moreover, the proposed approach does not depend on the converter architecture and can be applied to every A/D converter.

2 SYSTEM DESCRIPTION

Fig. 1 shows the transfer characteristic of an A/D converter. Design parameters are: the full-scale range, V_{max}, and the number of bits, N. From this, we can obtain an "A/D Fuzzifier" (ADF) through a non-linear transfer function, whose shape is triangular or trapezoidal. Fig. 2 illustrates an example of trapezoidal ADF

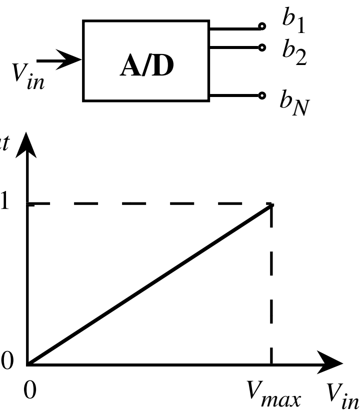

Fig. 1. Symbol and transfer characteristic of a conventional A/D converter.

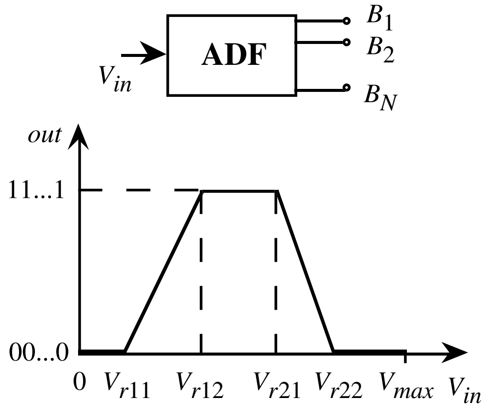

Fig. 2. Symbol and transfer characteristic of an "A/D fuzzifier" (ADF).

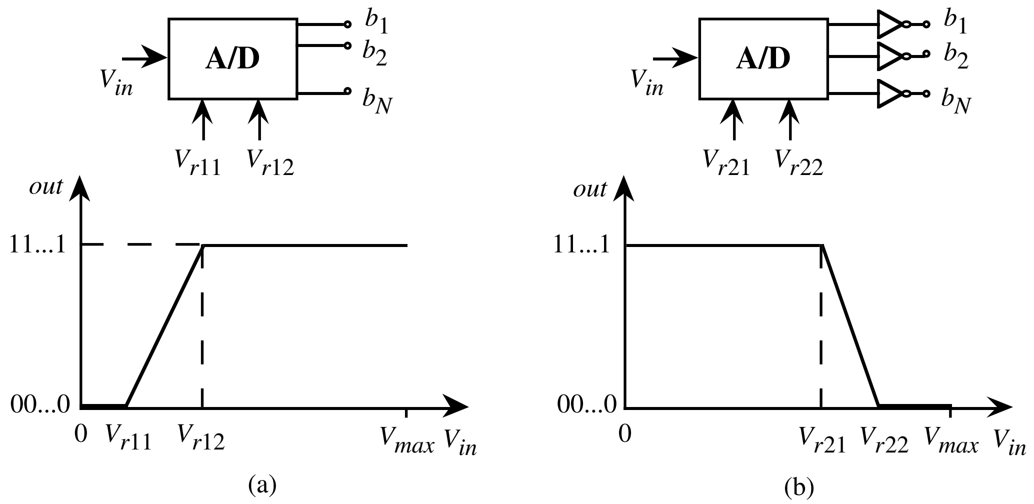

Fig. 3. Implementation of the membership function with two A/D converters.

characteristic. Instead of the full-scale range V_{max}, the ADF has four parameters, V_{r11}, V_{r12}, V_{r21} and V_{r22}, that define the slope and the offset of the two oblique edges, as shown in Fig. 2.

The first part (i. e., the rising edge) of the non-linear function can be obtained through a shifting and a compression of the A/D transfer characteristic in the interval $[V_{r11}, V_{r12}]$, as illustrated in Fig. 3(a). In the same way, through a compression in the interval $[V_{r21}, V_{r22}]$ and through a mirroring, we can obtain the second part (i. e., the falling edge) of the transfer characteristic shown in Fig. 3(b).

The ADF in Fig. 2 can be implemented with the general architecture shown in Fig. 4. Main blocks are: a conventional A/D converter with two reference inputs, the output block (COD), and a comparator that selects the A/D converter reference inputs and controls the COD. The COD inverts all bits according to the control signal C, and it can be as simple as shown in Fig. 5. When the input signal is lower than V_{r12}, reference voltages for the A/D converter are V_{r11} and V_{r12}, and the COD output is the A/D converter output unchanged; otherwise, the A/D converter reference voltages are V_{r21} and V_{r22}, and the COD complements the A/D converter output.

3 RESOLUTION IN FUZZY MEMBERSHIP FUNCTION

Let us suppose that the basic A/D converter is characterised by the following parameters: number of bits (N); input range (V_{max}); nominal quantisation step (Q) and differential non-linearity (D). The DNL D is the maximum difference between a real quantisation step and the ideal one, and is expressed in LSB units. Parameters N, V_{max} and Q are related through the relationship:

$$Q = \frac{V_{max}}{2^N - 1} . \tag{1}$$

In an ideal A/D converter, an input variation equal or larger than Q produces a change in the output code. On the other hand, in a real A/D converter the minimum resolution ΔV_{in} is limited by the error ΔQ in the quantisation step:

$$\Delta V_{in} = Q + \Delta Q . \tag{2}$$

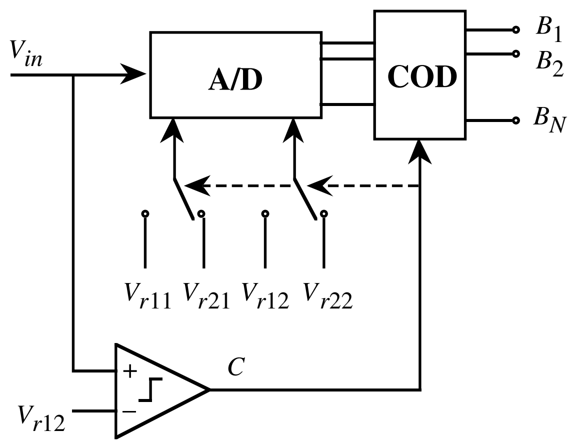

Fig. 4. General architecture of the A/D fuzzifier.

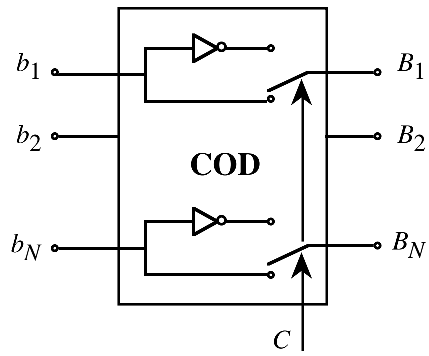

Fig. 5. Scheme of the COD block.

The term ΔQ is related to component non-idealities such as offset, noise, etc. and is independent on Q. ΔQ can be expressed as a function of the DNL D, according to the following relationship:

$$\Delta Q = D \cdot \frac{V_{max}}{2^N - 1}. \tag{3}$$

Combining (2) and (3), we obtain:

$$\Delta V_{in} = Q \cdot (1 + D). \tag{4}$$

In the ADF, the maximum slope in the input-output characteristics is achieved when the input voltage range is $\Delta V_r = \min(V_{r12} - V_{r11}, V_{r22} - V_{r21})$. In this case, the nominal quantisation step would be:

$$q = \frac{\Delta V_r}{2^N - 1}. \tag{5}$$

However, due to non-idealities of the A/D converter, to cause a change in the ADF digital output, the input variation should be:

$$\Delta V_{in} = q + \Delta Q = q \cdot \left(1 + D\frac{V_{max}}{\Delta V_r}\right). \tag{6}$$

By comparing (4) and (6), the differential non-linearity d of the ADF results to be:

$$d = D\frac{V_{max}}{\Delta V_r}. \tag{7}$$

For example, when an 8-bit converter with a DNL $D = 0.5$ is used to build an ADF with $\frac{V_{max}}{\Delta V_r} = 6$, the resulting DNL for the ADF is $d = 3$. Since d is larger than 1 LSB, the effective resolution of the ADF is less that the number of bits N.

From (6), we can see that the minimum quantisation step of the ADF, q_{min}, is limited by ΔQ:

$$q_{min} \geq \Delta Q \tag{8}$$

and the maximum resolution in bit of the ADF, N_{max}, is related to q_{min} according to:

$$q_{min} = \frac{\Delta V_r}{2^{N_{max}} - 1}. \tag{9}$$

Substituting (3) and (9) in (8), we get:

$$N_{max} \leq \frac{\ln\left(\frac{1}{D}\frac{\Delta V_r}{V_{max}}(2^N - 1) + 1\right)}{\ln 2} = $$

$$= \frac{\ln\left(\frac{2^N - 1}{d} + 1\right)}{\ln 2} \tag{10}$$

It is apparent that the maximum number of bits is limited by the DNL of the conventional A/D converter. Hence, the effective number of bit of the ADF, n, is:

$$n = \min(N, N_{max}). \tag{11}$$

In the above example, we get $N_{max} = 6$. Hence, the ADF equivalent resolution is limited to 6 bits, loosing two bits of resolution.

4 SIMULATION RESULTS

The proposed architecture of the ADF has been described in AHDL and simulated.

An ideal 4-bit A/D converter with $V_{max} = 5$ V, having the transfer characteristic shown in Fig. 6, has been used into an ADF with $V_{r11} = 0.5$ V, $V_{r12} = 2$ V, $V_{r21} = 3$ V and $V_{r22} = 3.75$ V. Fig. 7 shows the resulting transfer characteristic of the ADF.

To illustrate the effects due to the converter non-linearity, we have introduced a DNL $D = 0.5$ into the A/D converter, whose transfer characteristic is shown in Fig. 8. In this case, the resulting transfer characteristic of the ADF is shown in Fig. 9. According to (7), the DNL of the ADF is $d = 3.33$. From (10) we obtain $N_{max} = 2$, which

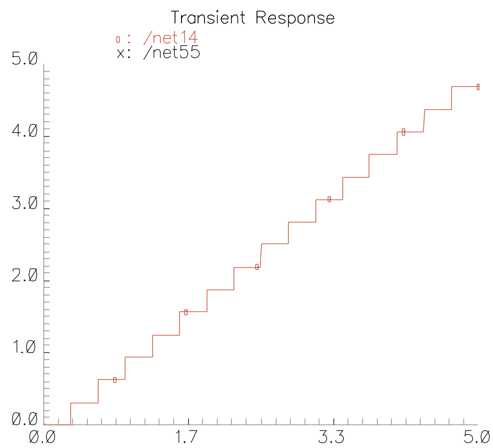

Fig. 6. Transfer characteristic of an ideal 4-bit A/D converter.

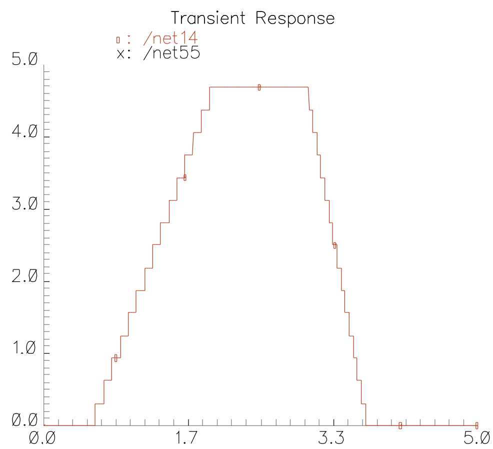

Fig. 7. Simulated transfer characteristic of the ADF made up with the ideal A/D converter.

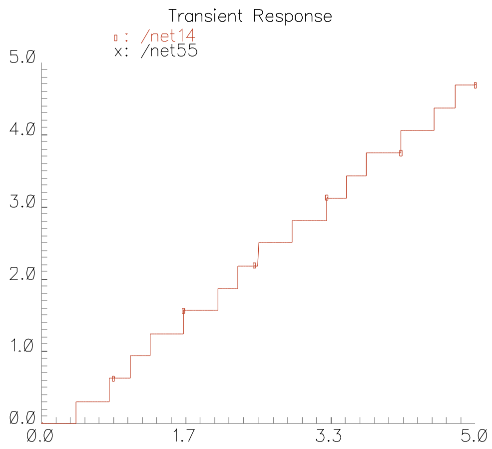

Fig. 8. Transfer characteristic of a 4-bit A/D converter with a DNL $D = 0.5$.

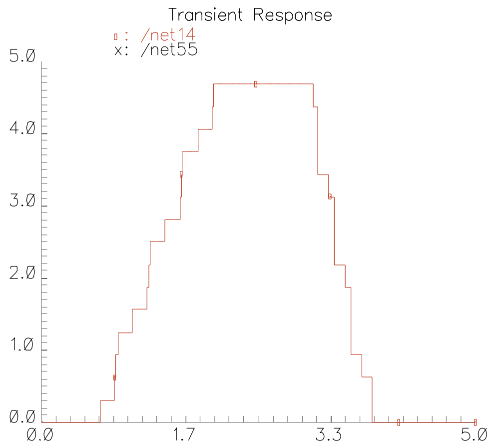

Fig. 9. Simulated transfer characteristic of the ADF made up with the A/D converter of Fig. 8.

means that the analog input signal is converted with only 2 bits of resolution when is lies of the ramp with maximum slope. For this ADF, only the two most significant bits should be taken into account for the fuzzy processing.

5 CONCLUSION

This paper has demonstrated that A/D conversion and fuzzy membership function can be merged into a single block, the A/D fuzzifier. A general and simple architecture to perform ADF has been presented. It is based on a conventional A/D converter and few other components, and is programmable by setting four reference voltages.

The use of this block reduces area and power consumption. A further saving in area and power consumption is possible by using only one ADF and multiplexing inputs and outputs in the realization of a fuzzy system.

The achievable resolution of the ADF has also been evaluated. The DNL and the effective number of bits of the resulting ADF have been related to the parameters of the conventional A/D converter adopted.

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