AN FPGA-BASED PHYSICAL LAYER IMPLEMENTATION FOR VEHICLE-TO-VEHICLE (V2V) COMMUNICATION

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ABSTRACT

This paper presents the design and implementation results for IEEE 802.11p Wireless Access in Vehicular Environment Physical layer using Field-Programmable Gate Array (FPGA) hardware. IEEE 802.11p defines modifications of IEEE 802.11a to support Intelligent Transportation Systems applications such as supporting public safety and licensed private operations over communication channels. Towards this objective our implementation goes through two phases. Firstly, a high-level design tool was used for the Forward Error Correction (FEC) coding chain. Xilinx System Generator is a system-level modeling tool that runs under MatLab Simulink and facilitates FPGA hardware design. Secondly, the use of Very High Speed Integrated Circuit Hardware Description Language (VHDL) was required for the design of the OFDM system. Finally the transmitter and the receiver were implemented into two identical FPGA boards provided by Nallatech using RF evaluation boards from Analog Devices in order to configure our system in 5.9 GHz.

1. INTRODUCTION

To begin with, in October 1999 the Federal Communications Commission (FCC), allocated the 5.9 GHz band for DSRC (Dedicated Short Range Communications) - based intelligent transportation systems (ITS) applications and adopted basic technical rules for DSRC operation. IEEE 802.11p standard has been endorsed by ASTM (American Society for Testing and Materials) [1] as the platform of the PHY and MAC layers for DSRC. The standard has been defined precisely for vehicular communications where high data transfer rates are required in circumstances where minimizing latency in the communication link is important. At first, the standard was designed for Vehicle to Infrastructure (V2I) systems but it was market demand that has caused the adaption with the V2V communications systems. The overall goal is the same: creating a network design useful for vehicle applications, but obviously taking into account the requirements of a safety system. Main purpose of the system is to provide drivers with real-time information beyond what is available through the senses alone. Furthermore, vehicular communication will offer a wide range of applications such as providing traffic management with a real time data for responding to road congestions.

FPGA devices are becoming a critical part of every system design and provide a flexible platform to accelerate performance-critical functions in hardware because of the configurability of the device's logic resources. The FPGAs are customized by loading configuration data into the internal memory cells.

Our contribution in this paper is to present the design and the implementation of the 802.11p physical layer in Radio Frequency zone. This work divides the design into two functional systems: the FEC coding chain and the OFDM system model. The former was designed using Xilinx System Generator design tool and the latter was designed using VHDL programming language. At the end the transceiver was targeted to Nallatech XtremeDsp Development Kit [2] with Virtex-4 FPGA provided by Xilinx and the configuration in 5.9GHz was carried out with RF evaluation boards from Analog Devices [3].

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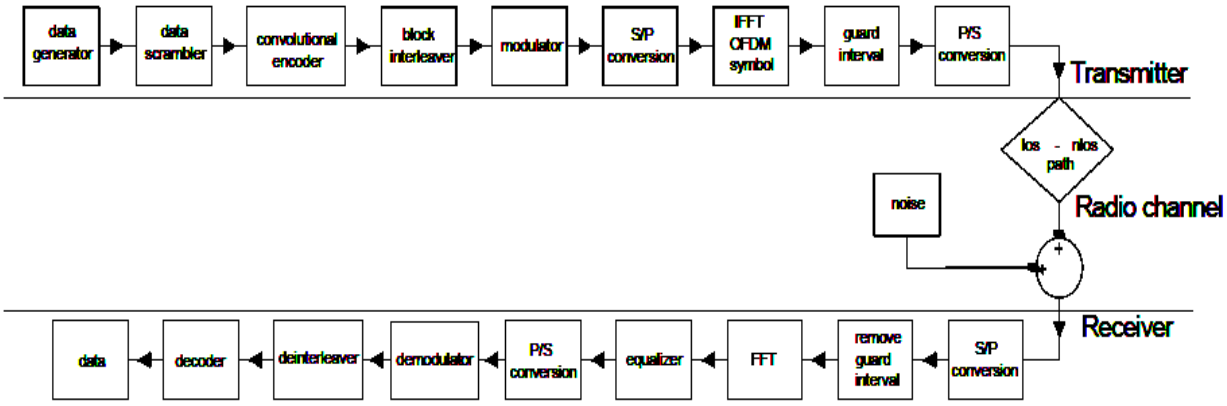

Figure 1 - IEEE 802.11p PHY block diagram

2. OFDM – IEEE 802.11P ARCHITECTURE

IEEE 802.11p standard specifies an OFDM Physical Layer (Fig. 1) that employs 64 subcarriers. 52 out of the 64 subcarriers are used for actual transmission consisting of 48 data subcarriers and 4 pilot subcarriers to provide transmission of data at rate 3, 4.5, 6, 9, 12, 18, 24, or 27 Mbps. The basic principal of operation is to divide a high-speed binary signal to be transmitted into a number of lower data rate subcarriers. The system uses pilot sub-carriers as a reference to disregard frequency or phase shifts of the signal during transmission. Orthogonality amongst the carriers is achieved by separating the carriers by an integer multiples of the inverse of symbol duration of the parallel bit streams. 802.11p specifies seven 10 MHz channels consisting of one control channel and six service channels. Four complex modulation methods (BPSK, QPSK, 16QAM, and 64QAM) are employed, depending on the data rate that can be supported by channel conditions. The maximum antenna input power for some DSRC mandatory channels is 28.8 dBm (750 mW) that enables long range.

The PHY layer structure of 802.11p standard is divided into two entities: the Physical Layer Convergence Protocol (PLCP) and the Physical Medium Dependent (PMD) sublayers. PLCP is one convergence procedure to map MAC PDU into a frame format designed for radio transceiver of corresponding PMD layer. PMD layer interacts with PLCP layer and provides the actual means to transmit data on medium.

3. FEC CODING CHAIN DESIGN

In this paper, we have used System Generator to generate VHDL source code from the Xilinx Blockset in Simulink environment for the FEC coding chain. Blocks from the Xilinx Blockset can be integrated seamlessly in Simulink models and are simulated in the same way. The tool provides high-level abstractions that are automatically compiled into an FPGA and access to underlying FPGA resources through low-level abstractions, allowing the construction of highly efficient FPGA designs.

We developed a model which is based on an OFDM Library v1.0 FEC Blockset and the WIMAX 802.16-2004 demonstration design kindly offered by Xilinx, and we have simulated Forward Error Correction Coding Chain of the transmitter and the receiver for 802.11p standard. After simulating the model, VHDL code was generated accordingly to our standard defined system parameters and synthesized for specific FPGA device. The coding chain (Fig. 2) of the transmitter consists of the following functional subsystems

- Randomizer
- Convolutional Encoder
- Interleaver
- Symbol Mapper

At the beginning data are imported serially into the data scrambler. The data scrambler using a 127 bits sequence generator scrambles all bits in the data field to randomize the bit patterns in order to avoid long streams of 1 and 0. After that, the data field shall be coded with a convolutional encoder of coding rate R = 1/2, 2/3, or 3/4, corresponding to the desired data rate. The output bits of the encoder are interleaved using the block interleaver within one OFDM symbol. The interleaved bits are then modulated using BPSK, QPSK, 16QAM, 64QAM modulator.

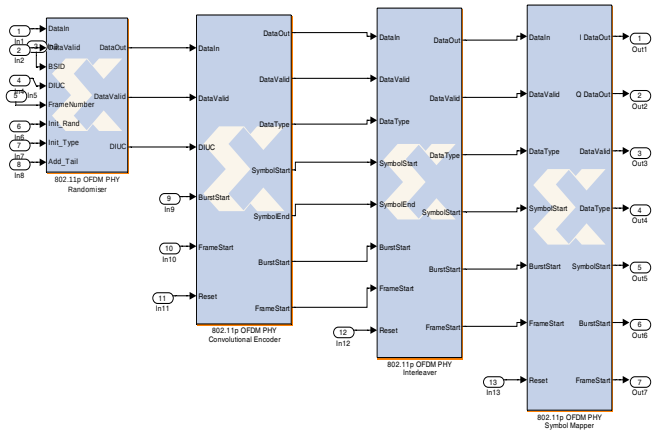

Figure 2 - IEEE 802.11p transmitter coding chain Xilinx Blockset

4. OFDM HARDWARE DESIGN

OFDM modulation is exploiting the fact that multiple data signals can be carried out from the same carry signal. The time space between the data signals which are carried from the carry signal is defined from the ratio $1/f_0$, where f_0 is the transmission duration of an OFDM symbol (symbol=wavelet). During the OFDM data modulation, every data sequence is considered to be available for transmission at any time and they are just separately distributed in the phase spectrum. Then, data spectrums are carried from the frequency to the time field through the inverse Fourier transform and they are transmitted in a wavelet sequence. During the OFDM demodulation, each wavelet is collected in serial sequence and after their transformation to parallel form, they are carried out into the frequency field through the Fourier transformation.

A crucial contribution in the modulation and demodulation procedure is given by the serial-to-parallel and parallel-to-serial modules. These modules are implemented in parallel.vhd and serial.vhd files respectively. The parallel component is converting serial data to parallel accepting as input sequential bits and producing bit arrays as output. Analogically, the parallel-to-serial component is using the same technique in order to accomplish the bit array to sequential bit transformation. Obviously, in order to implement the different digital data transmission through the same analog transmission signal, a transformation must be occurred so that the transmitted digital data could be safely carried through the carry signal. In this paper, the BPSK modulation is selected, created from the FEC coding chain mostly for simplicity and implementation reasons.

The main component of the OFDM project (Fig.3) is the modem component because it has the role of data receiver-transmitter but also the role of OFDM modulator-demodulator. The receiver - transmitter property is implemented with the coordination of three subcompoments: the txmodem, trx and the the rxmodem modules. The txmodem component is responsible for modulating data through the OFDM modulation and transmitting them. The rxmodem component is responsible for receiving data and demodulation them. Finally, the txrx component is responsible for the data passing through the BPSK modulator-demodulator and also for the communication with system's inputs and outputs.

The txmodem implementation is achieved with the presence of two submodules: the input component and the OFDM component. The input component is accepting the modulated through BPSK modulation data and passing them to the OFDM component. The OFDM component accepts the data coming from the input component as data bit arrays (12 bit length) and modulate the incoming data through OFDM modulation. The rxmodem module is operating in analogically way with the txmodem and it is consisted from the OFDM and the output subsystem. The OFDM subsystem is operating as a demodulator and the demodulated data are driven in the output subcomponent. The output subcomponent is responsible for the proper transfer of the OFDM demodulated data to the BPSK demodulator.

5. PHY FPGA IMPLEMENTATION

In hardware programming, XILINX ISE [4] software was used to perform the implementation. The Xilinx ISE system is an integrated design environment that that consists of a set of programs to create (capture), simulate and implement digital designs in a FPGA or CPLD target device. All the tools use a graphical user interface (GUI) that allows all programs to be executed from toolbars, menus or icons [5]. All the designs were targeted in two XtremeDSP Developments boards with Xilinx Virtex-4 XC4VSX35-10FF668 FPGA for the transmitter and the receiver respectively.

The XtremeDSP Development Kit-IV from Nallatech serves is an ideal development platform for the Virtex-4 FPGA technology and provides an entry into the scalable DIME-II systems. Its dual channel high performance ADCs and DACs, as well as the user programmable Virtex-4 device are ideal to implement high performance signal processing applications such as Software Defined Radio, 3G Wireless, Networking.

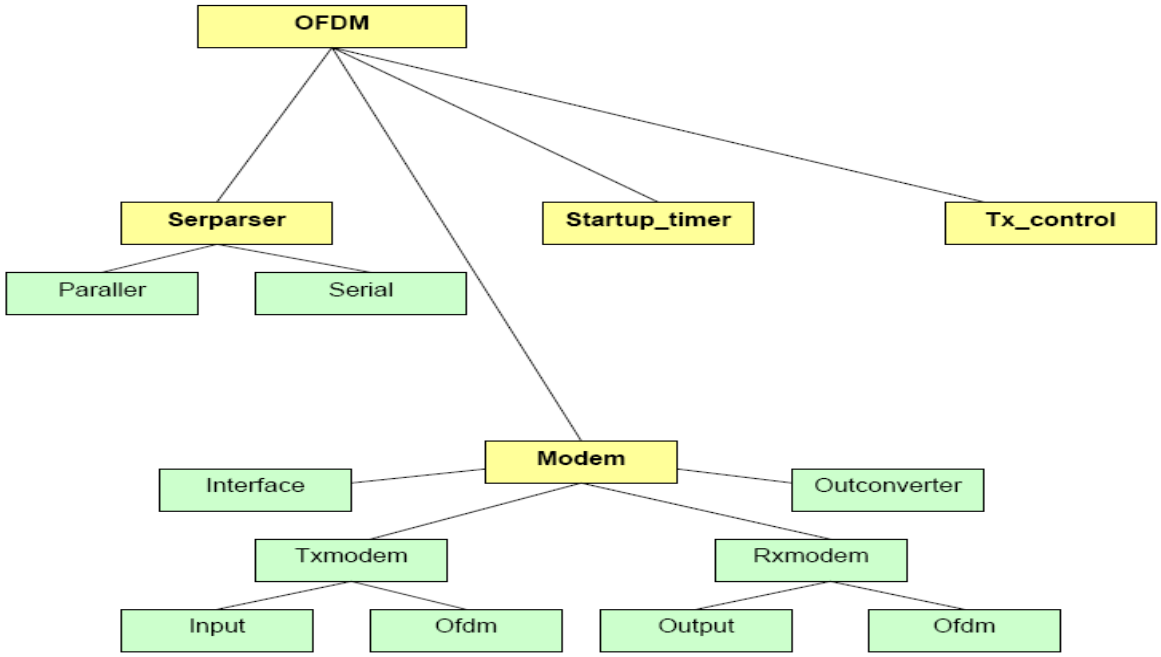

Figure 3 - OFDM schematic algorithm diagram

Nallatech's FUSE System Software [6] is a Java-based application that provides configuration, control and communications functionality between host systems and Nallatech FPGA computing hardware. This enables developers to design complex processing systems, with seamless integration between software, hardware and FPGA applications. FUSE provides several interfaces, including the FUSE Probe Tool which is ideal for configuration of the FPGA. The XtremeDSP Development Kit-IV features three Xilinx FPGAs - a Virtex-4 User FPGA, a Virtex-II FPGA for clock management and a Spartan-II Interface FPGA. The Virtex-4 device is available exclusively for user designs whilst the Spartan-II is supplied preconfigured with firmware for PCI/USB interfacing. The Virtex-4 XC4VSX35-10FF668 device is intended to be used for the main part of a user's design. The Virtex-II XC2V80-4CS144 is intended to be used as a clock configuration device in a design. To connect the development platform at the computer, three options exists, the Joint Test Action Group (JTAG) interface, the Universal Serial Bus (USB) and finally the Peripheral Component Interconnect (PCI) interface can be used. The User FPGA connects to this interface through the Interface FPGA.

Analog Devices offers several high-performance modulators and demodulators for operation at frequencies up to 6 GHz. ADL5375 [7] is a Broadband Quadrature Modulator designed for operation from 400 MHz to 6 GHz. Its excellent phase accuracy and amplitude balance enable high performance intermediate frequency or direct radio frequency modulation for communication systems. The ADL5380 [8] is a Broadband Quadrature I-Q demodulator that covers an RF/IF input frequency range from 400 MHz to 6 GHz. ADL5380 demodulator offers outstanding dynamic range suitable for the demanding infrastructure direct-conversion requirements. The differential RF inputs provide a well-behaved broadband input impedance of 50 Ω and are best driven from a 1:1 balun for optimum performance.

At the beginning the design run through synthesis, place and route stages, in ISE software and finally the programming bit file and the schematic symbols were generated. After that with FUSE software we located the XtremeDSP Motherboard through USB interface and finally we assigned two bitfiles to the devices for the Virtex-4 and Virtex-2 configuration. The test bed for the transmitter configuration is depicted in Fig 4. The outputs on the Fluke PM3380B oscilloscope for the input signal and the demodulated signal are depicted in Fig. 5 after connected the MCX-BNC cables from the DAC outputs on the board to channels on the oscilloscope. The development kit achieves a top frequency of 105 MHz which means t_{clk} = 9.5ns while utilizing 17% of the occupied slices, 13% of the D Flip-flops and 14% of the dedicated LUTs for the transmitter and the receiver.

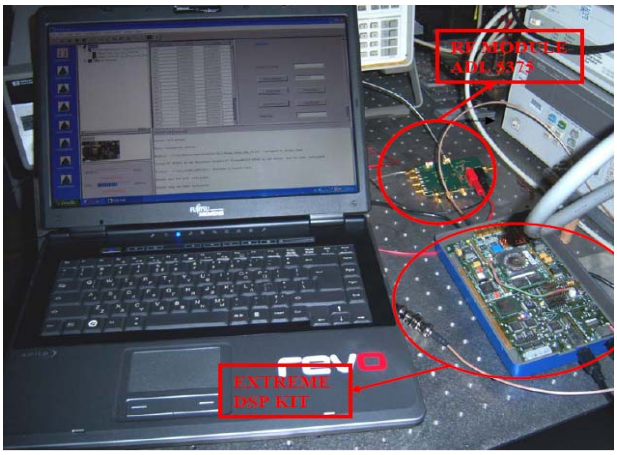

Figure 4 - Test bed using Nallatech XtremeDSP kit, Analog Device RF module and notebook with Fuse software for the transmitter configuration.

Implementation results for BPSK modulation with code rate ½ are shown in table I. Table I lists speed and resource usage (in terms of the building blocks of an FPGA) results under the following columns: a) Period, the critical path of the circuit in ns, b) LUT, the number of 4-input Look-Up Table function generators required, c) FF, the number of 1-bit flip-flops required, d) Slice, the number of FPGA slices required given that an FPGA slice has 2 LUTs and 2 FFs.

IMPLEMENTATION RESULTS	PERIOD	LUT	FF	SLICES
OFDM TRANSMITTER	14534ns	2944	2450	1882
OFDM RECEIVER	14628ns	3088	2566	1976

TABLE I – Implementation results for the transceiver

6. CONCLUSIONS AND FUTURE WORK

Taking everything into consideration, this article presents results regarding the design and the implementation of the transceiver for the IEEE 802.11p PHY. The transceiver was successfully developed using two identical Nallatech Development boards. Several modules have been designed and testing is required to obtain the result. Connecting the output of the transmitter to the input of the receiver the preliminary results shows high accuracy between measurements. In the future we intend to perform further experiments examining the 802.11p transceiver with different coding schemes such as Low Density Parity Check codes in order to enhance system performance. Extending this work we will develop the whole PHY transmitter and receiver with antennas for real time implementations in fading environment.

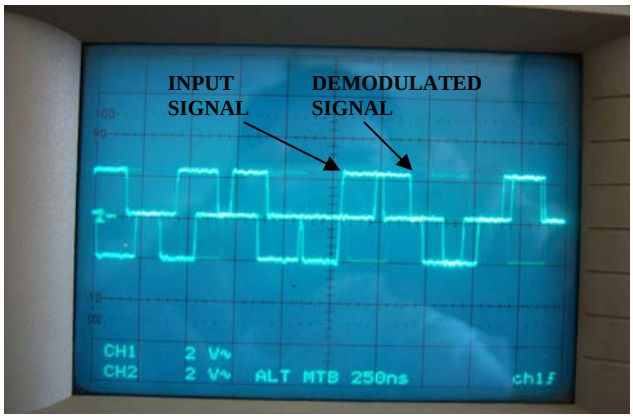

Figure 5 - Fluke PM3380B oscilloscope outputs. In channel 1is depicted the generator pulse and in channel 2 is depicted the demodulated signal

REFERENCES

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