

# Static Power Consumption Modeling and Measurement of Reconfigurable Intelligent Surfaces

Jinghe Wang, Wankai Tang, Shi Jin, Xiao Li, and Michail Matthaiou

**Abstract**—Reconfigurable intelligent surfaces (RISs) are anticipated to transform wireless communication in a way that is both economical and energy efficient. Revealing the practical power consumption characteristics of RISs can provide an essential toolkit for the optimal design of RIS-assisted wireless communication systems and energy efficiency performance evaluation. Based on our previous work that modeled the dynamic power consumption of RISs, we henceforth concentrate more on static power consumption. We first divide the RIS hardware into three basic parts: the FPGA control board, the drive circuits, and the RIS unit cells. The first two parts are mainly to be investigated and the last part has been modeled as the dynamic power consumption in the previous work. In this work, the power consumption of the FPGA control board is regarded as a constant value, however, that of the drive circuit is a variant that is affected by the number of control signals and its self-power consumption characteristics. Therefore, we model the power consumption of the drive circuits of various kinds of RISs, i.e., PIN diode-/Varactor diode-/RF switch-based RIS. Finally, the measurement results and typical value of static power consumption are illustrated and discussed.

**Index Terms**—Measurement, reconfigurable intelligent surface, static power consumption.

## I. INTRODUCTION

**F**UTURE wireless networks must contend with extremely complex networks, expensive hardware, and increasing energy consumption as the demands for wireless network capacity grow rapidly. In recent years, both the wireless research community and industry have paid close attention to the development of RISs, which can flexibly manipulate the electromagnetic properties of radio waves. Typically, a RIS is a 2D planar architecture that is made up of a large number of meticulously designed electromagnetic unit cells. The electromagnetic properties of these unit cells can be dynamically controlled by applying control signals, which create electromagnetic fields with controllable phase, amplitude, polarization, and frequency [1], [2]. Therefore, a RIS is introduced to enable the wireless propagation environment

J. Wang, W. Tang, S. Jin and X. Li are with the National Mobile Communications Research Laboratory, Southeast University, Nanjing 210096, China (e-mail: wangjh@seu.edu.cn; tangwk@seu.edu.cn; jinshi@seu.edu.cn; li\_xiao@seu.edu.cn). This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grants 62231009, 62261160576, and 62201138; the Natural Science Foundation of Jiangsu Province under Grant BK20220809.

M. Matthaiou is with the Centre for Wireless Innovation (CWI), Queen's University Belfast, Belfast BT3 9DT, U.K. (e-mail: m.matthaiou@qub.ac.uk). The work of M. Matthaiou was supported in part by the European Research Council (ERC) under the European Union's Horizon 2020 Research and Innovation Program under Agreement 101001331.

ISBN: 978-9-4645-9360-0

to change from passive adaptation to active control, thereby creating a smart radio environment [3].

When there not exists a direct link between the user equipment (UE) and the base station (BS), the RIS can be deployed to provide virtual line-of-sight (vLoS) links for signal transmission. The impinging signal is reflected by the RIS, and RIS performs 3D beamforming to improve the received signal quality by controlling the reflection phase shift of each RIS unit cell, which is expected to increase the wireless communication system's transmission rate, coverage, and energy efficiency. System performance enhancement can be achieved through joint active beamforming at the BS and passive beamforming at the RIS [4]–[8]. Moreover, the RIS prototyping system experimental validation and field trials were illustrated in [9]–[11]. These results are expected to pave the way for RIS deployments and practical use in the future.

The power consumption characteristic of RIS is also an essential topic. Revealing the practical power consumption characteristics of RISs can provide an essential toolkit for the optimal design of RIS-assisted wireless communication systems and energy efficiency performance evaluation. The authors in [6] and [12] developed power consumption models of RIS-assisted wireless communication systems which are mainly used for solving the energy efficiency optimization problems of RISs. However, the static power consumption of the FPGA control board and the drive circuit was not considered in [6], while the power consumption model of RIS was not illustrated in depth in [12]. The authors in [9] presented some initial measurement results on the RIS power consumption, which demonstrate that various RIS types have various power consumption characteristics. In [13], the power consumption of fabricated varactor-diode-based RIS was demonstrated. Nevertheless, the power consumption was not modeled and discussed thoroughly in [9], [13]. Against this background, we presented a precise RIS power consumption model. In [14], a quantitative relationship between the dynamic power consumption of the PIN-diode-based RIS and the polarization mode, controllable bit resolution, and working status of RIS was proposed, while the dynamic power consumption of the varactor-diode-based RIS was described to be almost negligible. Both conclusions were validated by practical experimental results. However, static power consumption is regarded as a constant part that is simply measured via power metering sockets, which should be analyzed more accurately.

Therefore, in this work, we complement the modeling of the static power consumption of RISs. Firstly, we divide the RIS hardware into three basic parts: the FPGA control board, the drive circuit, and the RIS unit cells. The first two parts are

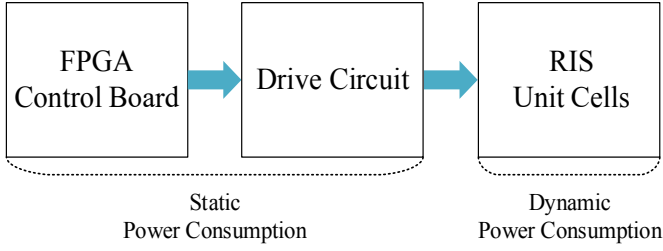


Fig. 1: General RIS hardware design structure can be simply divided into three parts: the FPGA control board, the drive circuit, and RIS unit cells.

mainly investigated in the following and the last part has been modeled as the dynamic power consumption in the previous work [14]. Particularly, the power consumption model of the drive circuits is proposed, which is affected by the number of control signals and its self-power consumption characteristics. Finally, various of fabricated RISs, i.e., PIN diode-/varactor diode-/RF switch-based RIS are introduced to illustrate the practical measurement results.

## II. STATIC POWER CONSUMPTION MODELING

RISs rely on adjustable electronic components, i.e., PIN diodes, varactor diodes, and RF switches to change the states of the RIS unit cells and perform 3D beamforming to refocus the energy from the incident RF signal to a specified direction. An external controller is required to be embedded in the RIS for programming, configuration, and digital control. As shown in Fig.1, general RIS hardware designs can be divided into three parts: the FPGA control board, the drive circuits, and RIS unit cells.

Firstly, the FPGA control board is a programmable array of logic gates, which is not only used for providing clock signals but also for data processing, i.e., generating the corresponding RIS beamforming coding sequence configuration according to the preset algorithm based on the feedback data information. Secondly, the drive circuits are used to drive the adjustable electronic components. They are usually integrated circuits for generating variable current/voltage according to the control signals from the master FPGA control board. Then, these adjustable electronic components are driven to achieve different coding states. At last, the RIS unit cells are artificial electromagnetic structures that are composed of substrates, metallic vias, metal patches, and adjustable electronic components. They are regularly arranged on a 2D surface and generate different 3D beamforming patterns according to the combination of different coding sequences.

Overall, the total power consumption dissipated to operate the RIS consists of two parts, one is the static power consumption generated by the FPGA control board and drive circuits, and the other is the dynamic power consumption generated by the RIS unit cells. Therefore, the total power consumption modeling of RIS can be expressed as follows:

$$P_{\text{RIS}} = P_{\text{static}} + P_{\text{dynamic}},$$

where  $P_{\text{static}}$  is the static power consumption and  $P_{\text{dynamic}}$  is the dynamic power consumption. In [14],  $P_{\text{dynamic}}$  has been precisely modeled. More specifically, for a PIN-diode-based RIS,  $P_{\text{dynamic}}$  is related to the number of RIS unit cells, the polarization mode, bit resolution, and the coding state of RIS unit cells. For the varactor-diode-based RIS,  $P_{\text{dynamic}}$  is almost zero, since the current in the varactor can be negligible when it works, even though the RIS unit cells are large in number. However,  $P_{\text{static}}$  has not been thoroughly investigated in [14]. According to whether the power consuming is affected by the number of control signals, the static power consumption dissipated to operate the RIS is the superposition of two parts, one is the power consumption of the FPGA control board  $P_{\text{control board}}$ , and the other is the power consumption of drive circuits  $P_{\text{total drive circuits}}$ . The static power consumption modeling of RIS can be expressed as follows:

$$P_{\text{static}} = P_{\text{control board}} + P_{\text{total drive circuits}}. \quad (2)$$

Generally, an FPGA selected as the master control board needs to have enough arithmetic power to cover all data processing, thus  $P_{\text{control board}}$  can be regarded as a constant value. However,  $P_{\text{total drive circuits}}$  is variable that is related to the types of adjustable electronic components, the number of control signals, and self-power consumption characteristics.

- $P_{\text{total drive circuits}}$  is related to the types of adjustable electronic components since different components utilize different types of drive circuits. For example, PIN-diode-based RIS unit cells can be driven by shift registers; varactor-diode-based RIS unit cells can be driven by digital-to-analog converters (DACs) and operational amplifiers (op-amps), PWM signals + level regulator [13], or CMOS logic circuits; RF switch-based RIS unit cells can be driven by FPGAs and shift registers.
- $P_{\text{total drive circuits}}$  is related to the number of control signals. Specifically, it is related to the number of adjustable electronic components  $N_c$  and the control Degree-Of-Freedom (DoF) of RIS (i.e., unit cell control, row control, column control, and sub-array control). RIS unit cells divided into the same group can use the same control signals, and  $N_g$  is denoted as the number of RIS unit cells that are in the same group with the same control signal.
- Total drive circuits are composed of multiple individual drive circuits. Therefore,  $P_{\text{total drive circuits}}$  is related to the self-power consumption characteristics of the individual drive circuit.  $N_s$  is denoted as the number of control signals generated by each drive circuit and  $P_{\text{drive circuit}}$  is denoted as the rated power consumption of a single drive circuit.

Based on the above,  $P_{\text{total drive circuits}}$  can be expanded as follows:

$$\begin{aligned} P_{\text{total drive circuits}} &= N_{\text{drive circuit}} \cdot P_{\text{drive circuit}} \\ &= \left\lceil \frac{N_c}{N_g \cdot N_s} \right\rceil \cdot P_{\text{drive circuit}}, \end{aligned} \quad (3)$$

where  $\lceil \cdot \rceil$  is the round-up symbol,  $N_c$  is the number of required adjustable electronic components,  $N_g$  is the number

$$P_{\text{static}} = \begin{cases} P_{\text{control board}} + \left[ \frac{\sum_{i=1}^N B_i}{N_g \cdot N_s} \right] \cdot P_{\text{drive circuit}}, & \text{PIN-diode/ RF switch-based RIS} \\ P_{\text{control board}} + \left[ \frac{N}{N_g \cdot N_s} \right] \cdot P_{\text{drive circuit}}, & \text{varactor-diode-based RIS} \end{cases} \quad (4)$$

of RIS unit cells that are in the same group with the same control signal, and  $N_s$  is the number of control signals generated by a single drive circuit. For PIN-diode-based RIS,  $N_c$  can be expressed by

$$N_c = \sum_{i=1}^N B_i, \quad (5)$$

where  $N$  is the number of RIS unit cells. Specifically, each PIN diode requires an input control signal to switch between 1 bit-binary state. Thus,  $B_i$  control signals are required for the  $i$ -th unit cell with  $B_i$  bits. For varactor-diode-based RIS, a single varactor can be coded to different states by applying different magnitudes of reverse bias voltage to it, thus  $N_c = N$ . For RF switch-based RIS, the  $i$ -th RF switch requires  $B_i$  control signals for  $B_i$ -bit coding states. Therefore,  $N_c$  is the same as PIN-diode-based RISs in (5). In conclusion,  $P_{\text{static}}$  is summarized as (4) at the top of this page. Equations (1), (4) in this work, and equation (2) in [14] form the full RIS power consumption modeling together.

### III. PRACTICAL STATIC POWER CONSUMPTION ANALYSIS

In the following section, we provide a detailed description and measurement results of the static power consumption of practical RISs. Overall, the FPGA control board is like the “brain” of the RIS, which needs to generate the coding sequences for regulating the RIS. A flow diagram for realizing a RIS triggered by the FPGA hardware is presented in Figure 7i in [1]. In the measured PIN-diode-based RIS and RF switch-based RIS, the FPGA XC7K70T is embedded as the master FPGA control board. With a working voltage of 24 V, its current is measured as 0.2 A. Therefore,  $P_{\text{control board}} = 4.8$  W. Some other FPGAs, i.e., Xilinx ZYNQ7100 are workable for simple RIS prototypes, which consume only 1.5 W like the RIS prototype in [13].

#### A. PIN-diode-based RIS

The RIS utilized for the first measurement belongs to the family of PIN-diode-based RIS, which is phase-programmable with 1-bit coding, as shown in Fig. 2. It can control the phase shift of reflected EM waves at the operating frequency  $f = 3.5$  GHz by unit cell independently. Four  $8 \times 8$  sub-RISs form a complete  $16 \times 16$  RIS. The PIN-diode drive circuits are essential since they affect the speed of the PIN diodes switching between “on/off” (coding states). By applying PIN-diode drive circuits, control signals from the FPGA master control board can be changed into output signals with current-driven capability. In the measured PIN-diode-based RIS, the SN74LV595A 8-bit shift registers are applied as drive circuits, as shown in Fig. 3.

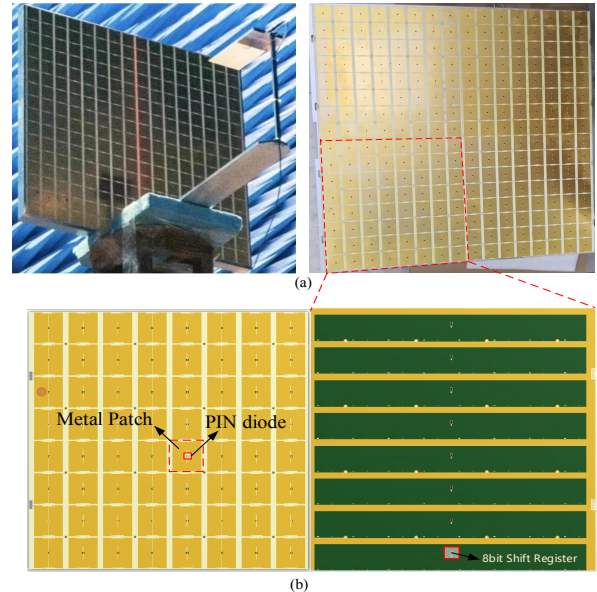


Fig. 2: Photograph of the fabricated PIN-diode-based RIS. (a) A complete  $16 \times 16$  RIS. (b) An  $8 \times 8$  sub-RIS structure.

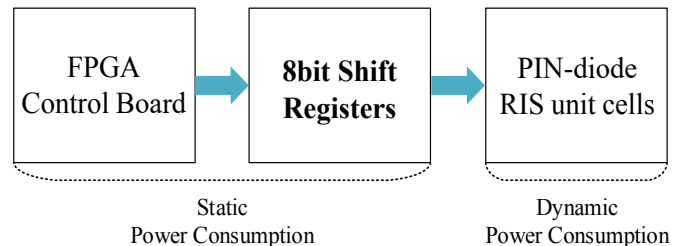


Fig. 3: The fabricated PIN-diode-based RIS hardware design structure.

Specifically, an 8-bit shift register is embedded for 8 RIS unit cells on a column in an  $8 \times 8$  sub-RIS. Therefore,  $8 \times 4 = 32$  shift registers are required in the complete  $16 \times 16$  RIS. When 8-bit shift registers are working at the voltage  $V_{cc} = 3.3$  V, the current we measured is  $I_{cc} = 20 \mu\text{A}$ , thus,  $P_{\text{drive circuit}} = 0.066$  mW. The key parameters of this RIS in the model are  $P_{\text{control board}} = 4.8$  W,  $N_c = 256$ ,  $N_g = 1$ ,  $N_s = 8$ , therefore  $N_{\text{drive circuit}} = 32$ , and  $P_{\text{total drive circuits}} = 32 \times P_{\text{drive circuit}} = 2.112$  mW. As illustrated in the measurement results, it can be seen that applying shift registers as drive circuits is an energy-efficient solution, ensuring that  $P_{\text{total drive circuits}}$  is about mW-level for hundreds/thousands of unit cells.

#### B. Varactor-diode-based RIS

The RIS utilized for the second measurement belongs to the family of varactor-diode-based RIS, as shown in Fig. 4(a).

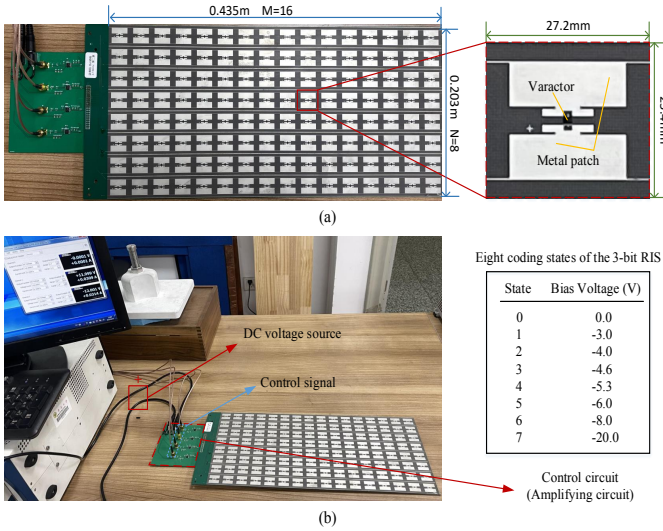


Fig. 4: Photograph of the fabricated varactor-diode-based RIS. (a) A complete RIS and its unit cell structure. (b) Practical measurement and a typical example of 8 coding states of the RIS.

It is operated at  $f = 3.2$  GHz by column control [15]. The RIS is composed of  $N = 8$  columns with  $M = 16$  RIS unit cells in each column. The varactor diodes are embedded to bridge the metal patches and operated as an adjustable device and are operated under reverse bias voltages. The typical 8 coding states corresponding to the bias voltages applied on the varactors are illustrated in Fig. 4(b). Varactor-diode-based RIS unit cells can be driven by DAC + op-amp, PWM signals + level regulator, or CMOS logic circuits. In the measured varactor-diode-based RIS, the DAC and op-amp are applied, as shown in Fig. 5. DACs take digital inputs and generate analog outputs that provide bias voltages of varactor diodes. However, the bias voltage generated by the common DAC is usually low and can not achieve a high one like -20 V in Fig. 4(b). Therefore, the op-amp is necessary for the operation amplification function. Moreover, the DAC3484 is applied as a DAC, and the AD8021 low-noise, high-speed amplifier is applied as an op-amp.

In our measurement, 2 columns of RIS unit cells are in the same group with the same control signal, thus  $N_g = 16 \times 2 = 32$ . Specifically, DAC3484 consumes about 250 mW for generating one signal. When the AD8021 works at the voltage  $V_{cc} = \pm 12$  V, the current we measured is 7.5 mA, so the power consumption of the AD8021 is 180 mW. Thus,  $P_{\text{drive circuit}} = 250 + 180 = 430$  mW. The key parameters of this RIS in the model are  $N_c = 128$ ,  $N_g = 32$ , and  $N_s = 1$ , therefore  $N_{\text{drive circuit}} = 4$ , and  $P_{\text{total drive circuits}} = 4 \times P_{\text{drive circuit}} = 1720$  mW.

### C. RF Switch-based RIS

Common solutions implement PIN-diode-based RISs with a finite-bit resolution phase shift and implement varactor-diode-based RISs with both discrete and continuous control of the phase shift. Recently, RF switch-based RISs have emerged,

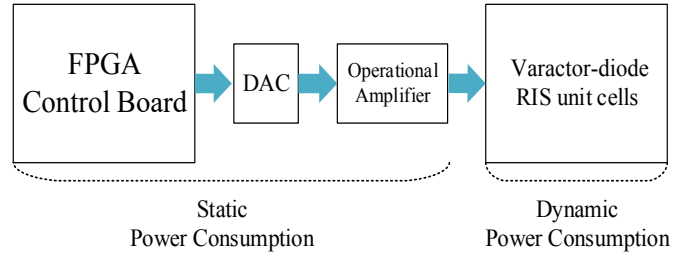


Fig. 5: The fabricated varactor-diode-based RIS hardware design structure.

since their implementations entail low costs [16]. Not only that, in addition to producing phase shifts onto impinging signals in a programmable manner, an RF switch-based RIS can configure individual cells to fully absorb the energy of RF signals, which provides open several opportunities. The RIS utilized for the third measurement belongs to the family of RF switch-based RIS, as shown in Fig. 6 and it is composed of  $8 \times 8 = 64$  RIS unit cells, with each unit cell being regulated independently. A RIS unit cell consists of an RF CMOS switch embedded in the metal patch. For an RF switch-based RIS, RF switch drivers are needed to provide logic levels to control the RF switches switching between different coding states, as shown in Fig. 7.

In the measured RF switch-based RIS, FPGA XC3S400AN is embedded as an RF switch driver to control 64 RIS unit cells. When FPGA XC3S400AN is working at the voltage  $V_{cc} = 12$  V, the current is measured as 20 mA. Therefore,  $P_{\text{drive circuit}} = 240$  mW. The key parameters of this RIS in the model are  $N_c = 64$ ,  $N_g = 1$ , and  $N_s = 75$  (a single FPGA XC3S400AN can control about 75 RF switches), therefore  $N_{\text{drive circuit}} = 1$ , and  $P_{\text{total drive circuits}} = P_{\text{drive circuit}} = 240$  mW.

### D. Discussion

The power consumption of various RISs is discussed and summarized in the following. The results are all supported by practical measurements.

The FPGA control board consumes Watt-level power for data processing. For the PIN-diode-based RISs, the drive circuits of PIN-diode-based RIS are energy-efficient, which is mWatt-level consuming, like  $P_{\text{drive circuit}} = 0.066$  mW for each 8-bit shift register and  $0.066/8 = 8 \times 10^{-3}$  mW for each control signal. However, the  $P_{\text{dynamic}}$  of PIN-diode-based RIS can be very large. In [14], the  $P_{\text{PIN}}$  of each unit cell in 1<sup>#</sup> RIS is measured as 12.6 mW, and the maximum  $P_{\text{dynamic}}$  is about 90 W when all unit cells are encoded as "1".

For the Varactor-diode-based RISs, even though the  $P_{\text{dynamic}}$  of varactor-diode-based RIS is almost zero, the drive circuits of it are often much more complicated and energy-hungry, like  $P_{\text{drive circuit}} = 430$  mW for each control signal with continuous bias voltage variation. Nevertheless, discrete-type varactor-diode-based RISs are promising for energy-efficient design, since its  $P_{\text{dynamic}}$  is almost zero and its drive circuit  $P_{\text{total drive circuits}}$  may sharply decline for only generating discrete-level bias voltage. Moreover, there still remain chal-

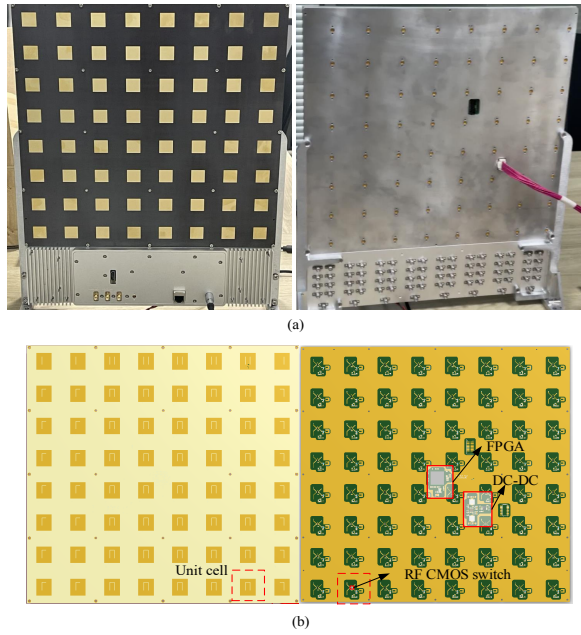


Fig. 6: Photograph of the fabricated RF switch-based RIS. (a) A complete RIS physical diagram. (b).  $8 \times 8$  RIS structure and parameters' illustration.

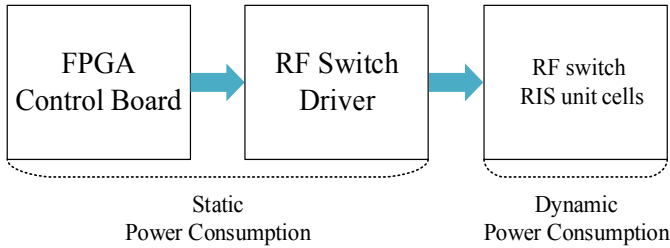


Fig. 7: The fabricated RF switch-based RIS hardware design.

challenges for designing and manufacturing the varactor-diode-based RIS in high-frequency bands (e.g., mmWave band).

For the RF switch-based RISs, the  $P_{\text{total drive circuits}}$  of RF switch-based RISs is measured as 240 mW for a single drive circuit (FPGA) to control 64 unit cells and  $240/64 = 3.75$  mW for each control signal. Actually,  $P_{\text{total drive circuits}}$  can be further reduced for the low power consumption design. For example, shift registers can also be utilized as RF switch drivers, in which the  $P_{\text{total drive circuits}}$  of RF switch-based RISs is comparable to that of PIN-diode-based RISs. Additionally, the  $P_{\text{dynamic}}$  of RF switch-based RISs is usually  $\mu\text{Watt}$ -level power-consuming, about  $3.3 \text{ V} \times 150 \mu\text{A} = 495 \mu\text{W}$  for each unit cell. Overall, the low power consumption design of RISs is an open research area for further investigation.

#### IV. CONCLUSION

In this work, we divided the RIS hardware into three basic parts: the FPGA control board, the drive circuits, and the RIS unit cells. The previous work has modeled the dynamic power consumption of RIS unit cells, thus we investigated the static power consumption of the FPGA control board  $P_{\text{control board}}$  and that of the drive circuits  $P_{\text{total drive circuits}}$ . We articulated

that the  $P_{\text{control board}}$  can be regarded as a constant value and  $P_{\text{total drive circuits}}$  is affected by the number of control signals and its self-power consumption characteristics. Particularly,  $P_{\text{total drive circuits}}$  is modeled for various kinds of RIS, i.e., PIN diode-/Varactor diode-/RF switch-based RIS, and measurement results validated the model of  $P_{\text{static}}$ . Overall, the dynamic power consumption modeling  $P_{\text{dynamic}}$  in the previous work in [14] and the static power consumption modeling  $P_{\text{static}}$  in this work form the full RIS power consumption modeling together.

#### REFERENCES

- [1] T. J. Cui, M. Q. Qi, X. Wan, J. Zhao, and Q. Cheng, "Coding metamaterials, digital metamaterials and programmable metamaterials," *Light Sci. Appl.*, vol. 3, no. 10, p. e218, Oct. 2014.
- [2] L. Zhang, X. Q. Chen, R. W. Shao, J. Y. Dai, Q. Cheng, G. Castaldi, V. Galdi, and T. J. Cui, "Breaking reciprocity with space-time-coding digital metasurfaces," *Adv. Mater.*, vol. 31, no. 41, p. 1904069, Aug. 2019.
- [3] M. D. Renzo, M. Debbah, D.-T. Phan-Huy, A. Zappone, M.-S. Alouini, C. Yuen, V. Sciancalepore, G. C. Alexandropoulos, J. Hoydis, H. Gacanin *et al.*, "Smart radio environments empowered by reconfigurable AI meta-surfaces: An idea whose time has come," *EURASIP J. Wireless Commun. Netw.*, vol. 2019, no. 1, pp. 1–20, 2019.
- [4] Y. Han, W. Tang, S. Jin, C.-K. Wen, and X. Ma, "Large intelligent surface-assisted wireless communication exploiting statistical CSI," *IEEE Trans. Veh. Technol.*, vol. 68, no. 8, pp. 8238–8242, Aug. 2019.
- [5] Q. Wu and R. Zhang, "Intelligent reflecting surface enhanced wireless network via joint active and passive beamforming," *IEEE Trans. Wireless Commun.*, vol. 18, no. 11, pp. 5394–5409, Nov. 2019.
- [6] C. Huang, A. Zappone, G. C. Alexandropoulos, M. Debbah, and C. Yuen, "Reconfigurable intelligent surfaces for energy efficiency in wireless communication," *IEEE Trans. Wireless Commun.*, vol. 18, no. 8, pp. 4157–4170, Aug. 2019.
- [7] K. Feng, Q. Wang, X. Li, and C.-K. Wen, "Deep reinforcement learning based intelligent reflecting surface optimization for MISO communication systems," *IEEE Wireless Commun. Lett.*, vol. 9, no. 5, pp. 745–749, 2020.
- [8] K. Feng, X. Li, Y. Han, and Y. Chen, "Joint beamforming optimization for reconfigurable intelligent surface-enabled MISO-OFDM systems," *China Commun.*, vol. 18, no. 3, pp. 63–79, 2021.
- [9] W. Tang, M. Z. Chen, X. Chen, J. Y. Dai, Y. Han, M. Di Renzo, Y. Zeng, S. Jin, Q. Cheng, and T. J. Cui, "Wireless communications with reconfigurable intelligent surface: Path loss modeling and experimental measurement," *IEEE Trans. Wireless Commun.*, vol. 20, no. 1, pp. 421–439, Jan. 2020.
- [10] G. C. Trichopoulos, P. Theofanopoulos, B. Kashyap, A. Shekhawat, A. Modi, T. Osman, S. Kumar, A. Sengar, A. Chang, and A. Alkhateeb, "Design and evaluation of reconfigurable intelligent surfaces in real-world environment," *IEEE Open J. Comm. Soc.*, vol. 3, pp. 462–474, Mar. 2022.
- [11] J. Sang, Y. Yuan, W. Tang, Y. Li, X. Li, S. Jin, Q. Cheng, and T. J. Cui, "Coverage enhancement by deploying ris in 5G commercial mobile networks: Field trials," *IEEE Wireless Commun.*, pp. 1–21, Dec. 2022.
- [12] A. Zappone, M. Di Renzo, F. Shams, X. Qian, and M. Debbah, "Overhead-aware design of reconfigurable intelligent surfaces in smart radio environments," *IEEE Trans. Wireless Commun.*, vol. 20, no. 1, pp. 126–141, Jan. 2020.
- [13] X. Pei, H. Yin, L. Tan, L. Cao, Z. Li, K. Wang, K. Zhang, and E. Björnson, "Ris-aided wireless communications: Prototyping, adaptive beamforming, and indoor/outdoor field trials," *IEEE Trans. Commun.*, vol. 69, no. 12, pp. 8627–8640, Dec. 2021.
- [14] J. Wang, W. Tang, J. C. Liang, L. Zhang, J. Y. Dai, X. Li, S. Jin, Q. Cheng, and T. J. Cui, "Reconfigurable intelligent surface: Power consumption modeling and practical measurement validation," *arXiv preprint arXiv:2211.00323*, 2022.
- [15] J. C. Liang, Q. Cheng, Y. Gao, C. Xiao, S. Gao, L. Zhang, S. Jin, and T. J. Cui, "An angle-insensitive 3-bit reconfigurable intelligent surface," *IEEE Trans. Antennas Propag.*, vol. 70, no. 10, pp. 8798–8808, Oct. 2021.
- [16] M. Rossanese, P. Mursia, A. Garcia-Saavedra, V. Sciancalepore, A. Asadi, and X. Costa-Perez, "Designing, building, and characterizing rf switch-based reconfigurable intelligent surfaces," in *Proc. the 16th ACM Workshop on Wireless Network Testbeds, Experimental evaluation & Characterization*, Oct. 2022, pp. 69–76.