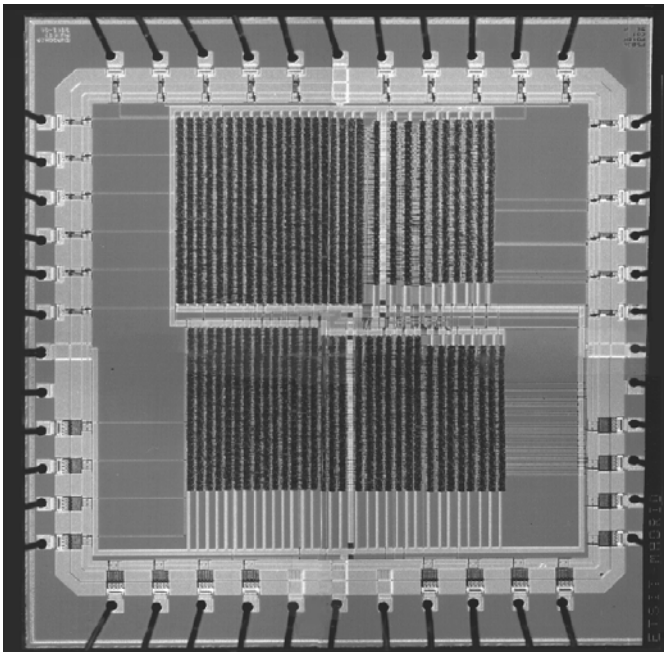

Low-Power Design (LPD)

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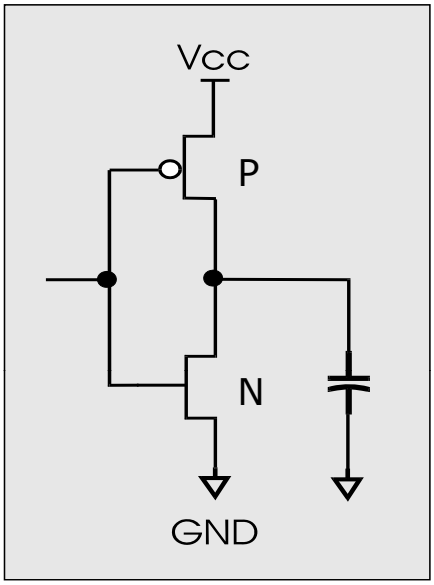
Dynamic Power = c f V^2

Σ Node capacitance x Node frequency x Node Voltage^2



0→ 1: $Energy_{cap} = 1/2\ C\ V^2$

$Energy_{tota\ l} = C\ V^2$

$Energy_{P\text{-}tran} = 1/2\ C\ V^2$

1→ 0: $Energy_{N\text{-}tran} = 1/2\ C\ V^2$

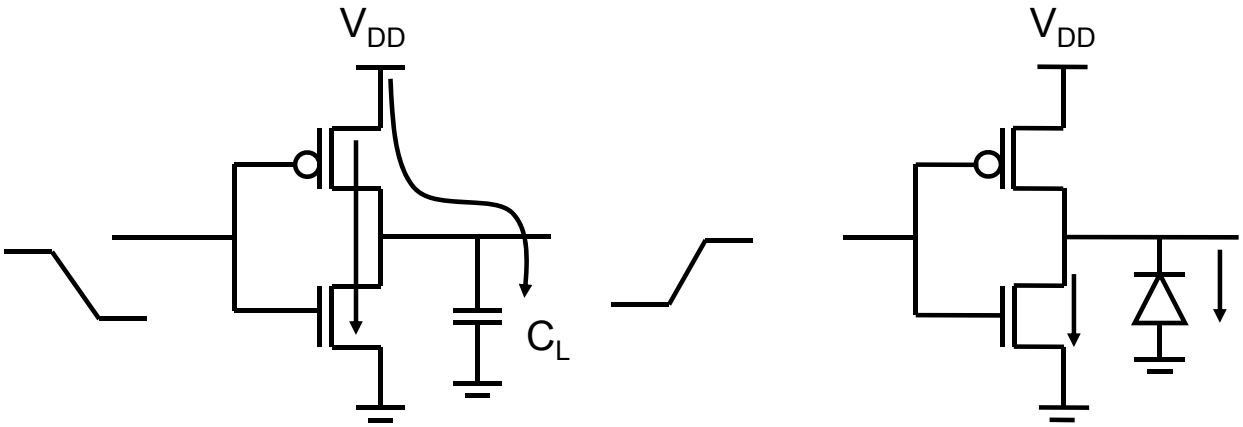
Dynamic Power:

$P = Energy / Time = E \cdot f = C.f.V^2$

(if the node reach V and GND completely)

Other power components: Dynamic … + Short Circuit + Leakage

$$P_{total} = C_L f V_{DD}^2 + V_{DD} I_{sc} + V_{DD} I_{leakage}$$

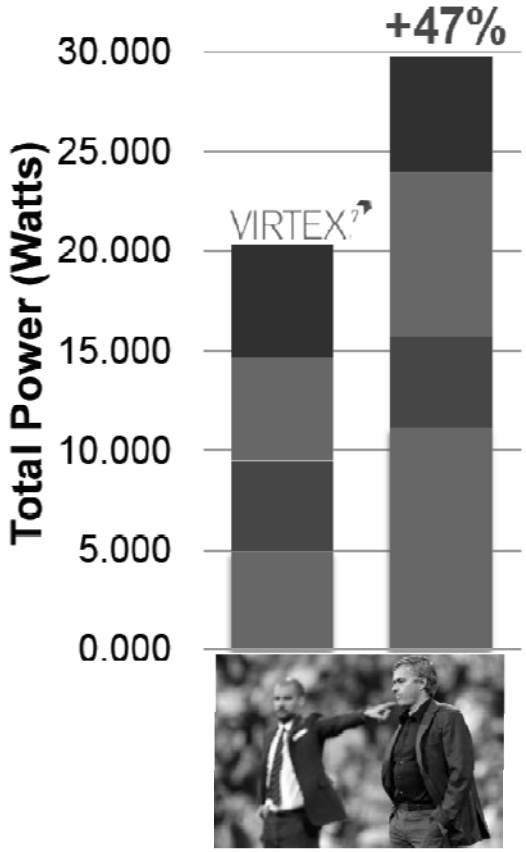


Source: http://www.eng.auburn.edu/~vagrawal

Power components: Structural classification

- ***Dynamic Power:***
  - ***Clock power*:** Power in the clock tree and FFs.
  - ***Off-chip power*:** Power in the output *pads*. Off-chip capacitances are 1000 times bigger. Is not a function of the FPGA model.
  - ***Datapath power*:** Power of the logic that process the data.
- ***Static Power:*** DC Power (*f*clk=0)
  - Raw FPGA.
  - Configured FPGA.
- Configuration power.

Power Figure in 2012 FPGAs



- **Example:**
  - Traffic Manager in 100G Line Card Virtex-7 VX550T .
  - Source: 7-series-power-benchmark-summary.pdf **Xilinx Inc**, Dec 2012

Dynamic Power: Effective frequency

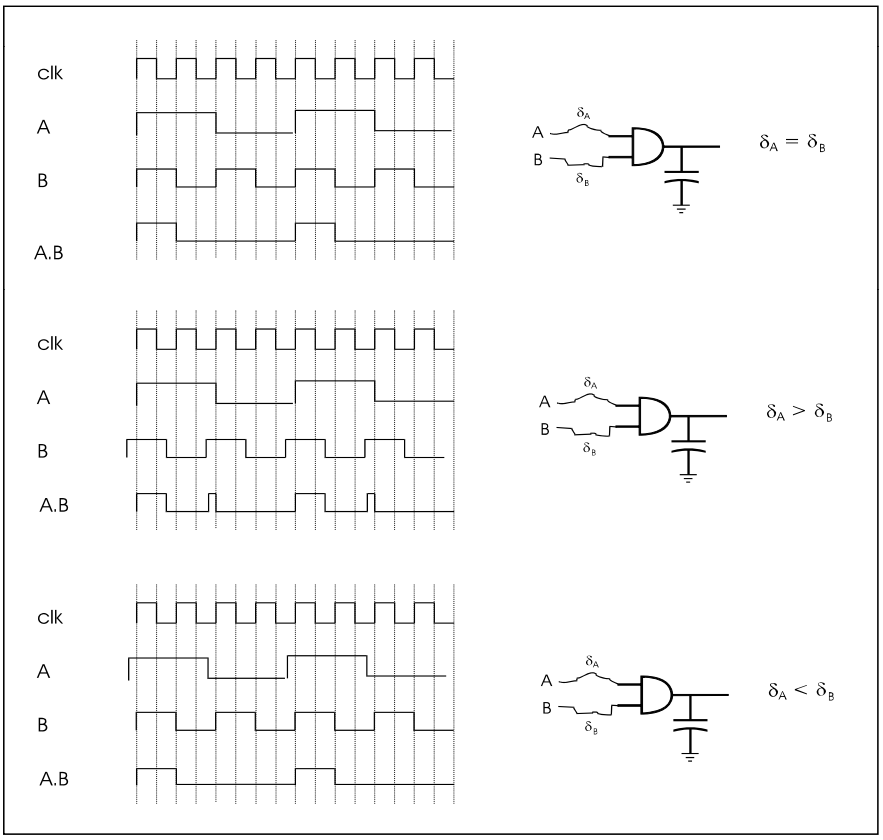
- The f is the frequency of each node (not system f_{CLK}).
- There is an activity factor $f = \alpha f_{CLK}$
- The activity factor depend on the **logic functions** and the **input data**

A	B	A.B	A+B	A⊕B
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

Example

Prob $_{0\text{-}1} = P_0.P_1$ is different in each case

Dynamic Power: Effective frequency and *glitches*



- *Glitches* are spurious transitions due to different delays.
- *Glitches* generate activity producing a snow-ball effect
- In FPGA technology glitch power depend on the PPR.
- The contribution of glitches to the total power is huge.

Xilinx strategies to minimize dynamic power

Table 4: **Dynamic Power Reduction Techniques in Virtex-6 and Spartan-6 FPGAs**

Reduction Technique	Power Savings	Reason for Xilinx Choice
Smaller process	Approximately linear reduction in dynamic power in the core based on transistor and interconnect shrink.	Allows packing more transistors into a given area to increase density.
Clock gating enhancements	Depends on clock enable duty cycle (10–80% can be achieved).	Offers an excellent opportunity for customers and software to reduce clock-tree power.
LUT4 vs. LUT6	Approximately 15–20%. Since the logic of the design can be kept in less logic, the design requires less area and fewer interconnects. Both lower capacitance.	Offers higher performance, smaller area, and less total transistors needed to build a programmable logic function.
Tool support for block RAM low-power modes	Up to 75% reduction in dynamic power.	Many customers make large arrays of block RAM and Xilinx wanted to offer an easy way to choose power or area-based trade-offs.
Integrated blocks	Up to 90% reduction in dynamic power compared to soft-IP implementations.	Selecting a set of common blocks needed by many customers allows Xilinx to offer better performance and lower static and dynamic power.
Voltage scaling (-1L devices)	Dynamic power is proportional to V_{CCINT}^2 (i.e., ~19% reduction for 10% lower V_{CCINT}).	Up front IC design verification and implementation of process screen at manufacturing test allows lower power option for users.

Xilinx strategies to minimize static power

Table 1: **Static Power Reduction Techniques Used in Spartan-6 and Virtex-6 FPGAs**

Reduction Technique	Power Savings	Reason for Xilinx Choice
Transistor distribution optimizations in integrated blocks and core logic	25–90% reduction depending on block vs. less judicious use of Low V_T transistors in previous generation devices.	Great reduction in leakage by Xilinx investment at design time.
Middle thickness oxide transistor used in configuration memory and interconnects (triple-oxide approach)	Greater than 40% reduction vs. thin oxide.	Great reduction in leakage by Xilinx investment at design time.
User-controllable suspend feature for low power or battery-based applications	30% reduction vs. normal lowest operational leakage state.	System-level power management values brought to customer—useful for system-level power management in high volume applications.
User-based shutdown/wakeup of PLLs	Saves DC and AC operating power of PLLs when system allows wakeup/sleep of a PLL.	User flexibility for live in-design reduction of power.
Partial reconfiguration	80% static power savings if several sections of logic are swapped in and out of the active design.	Unique Xilinx benefit; great static power savings.
Integrated blocks	Up to 90% reduction in static power compared to soft-IP implementations.	Selecting a set of common blocks needed by many customers allows Xilinx to offer better performance and lower static and dynamic power.
Voltage scaling (-1L devices only)	Static power from leakage goes as ~V_{CCINT}^3 (i.e., ~27% reduction for 10% lower V_{CCINT}).	Up-front IC design verification and implementation of process screen at manufacturing test allows lower power option for users.

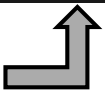
Off-chip Power

XILINX

Dynamic Power Consumption

	XC3042	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.07	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	0.50	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	0.55	1.25	mW per MHz

- 1985 databook



- **C x f x V²** = 50 pF x f x 25 v^2 = 1250 10^{-12} 10^6 x f [MH]

  watts/MHz = 1,25 mW/MHz
- The off-chip power (pins) does not depend on –excepting V - the scale integration. It is simply caused by 2 transistors (inside the chip) that charge/descharge a capacitance (outside the chip).

Off-chip power: Xilinx LPD strategies

Table 8: **I/O Power Reduction Techniques**

Reduction Technique	Benefit	Reason for Xilinx Choice
Programmable slew rate and drive strength. Use the lowest slew/power to get the job done.	Lowers dynamic power in I/O drive.	Gives user the ability to choose various edge rates for signal integrity vs. I/O dynamic power.
3-stateable DCI	Dynamically assertable termination during memory read removes termination power during memory write.	Eliminates unnecessary termination power when I/O input is not being used.
HSLVDCI series termination	50% input power reduction for FPGA inputs driven by HSLVDCI vs. split termination plus IODELAY plus input buffer power (i.e., split termination is removed).	Offers users the ability to gain a high-performance, single-ended I/O standard and lower power without the need for a parallel termination.
Programmable IODELAY power Low power or highest performance	70% input power reduction vs. high performance.	Offers the user the ability to selectively, at their choice, reduce IODELAY power for small reduction in performance.
Programmable reference receiver power (HSTL, SSTL, LVDS) Low power or highest performance	50% input power reduction vs. high performance.	Offers the user the ability to selectively, at their choice, reduce power for the input receiver for a small reduction in performance.

Discussion: slew-rate, driving capability, power, and energy.

Synchronization power : Current FPGAs

FPGA Comparison Table

Features	Artix-7	Kintex-7	Virtex-7	Spartan-6	Virtex-6
Logic Cells	352,000	480,000	2,000,000	150,000	760,000
BlockRAM	19Mb	34Mb	68Mb	4.8Mb	38Mb
DSP Slices	1,040				2,016

Part Number	XC7VX1140T
EasyPath™ Cost Reduction Solutions(1)	XCE7VX1140T
Slices(2)	178,000
Logic Cells(3)	1,139,200
CLB Flip-Flops	1,424,000

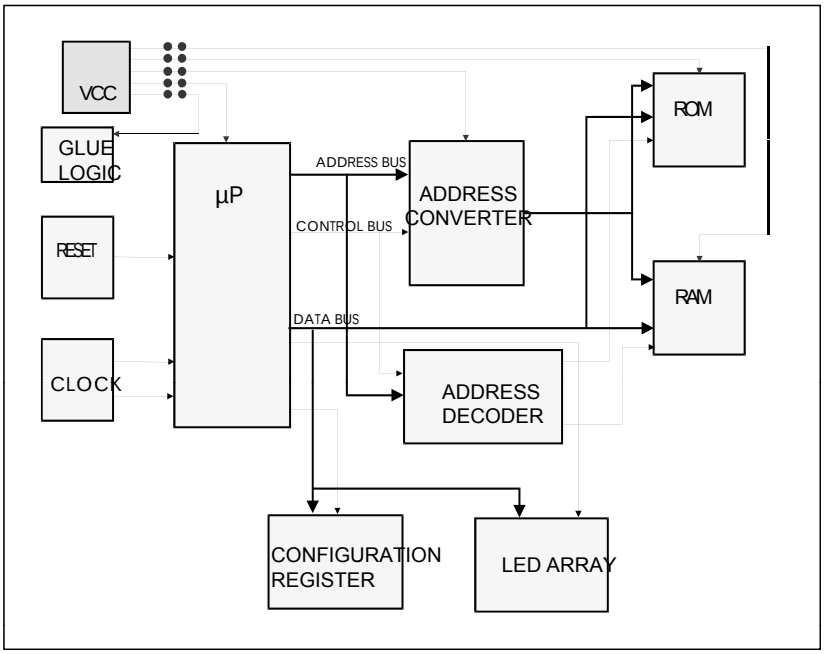
- High-speed → Pipelining → great number of registers
- Registers conmute at f_{Clock} (if clock gating is not applied)
- The sinchronization power is a linear function of the product #FF x $f_{CLK.}$

Power analysis and measurement at system level

- PCB must be designed with some of the following characteristics:
  - Power supply terminals must be accessible and separated.
    - In commercial board is possible to overcome this problem removing the voltage regulators.
  - Possibility of stop/replace clock signal.
  - "Separativity" of power supply by functional blocks.
  - External control of different chip output-enable signals.
    - Scaling in frequency is possible.

Power analysis and measurement at system level

Source: G. Gonzalez de Rivera, J. Garrido, and E. Boemo, "Power Audit of an Space-Certified Microprocessor", *Proc PATMOS'99 (International Workshop Power and Timing Modeling, Optimization and Simulation)*, pp.551-556, October 6-8, Kos Island, Greece

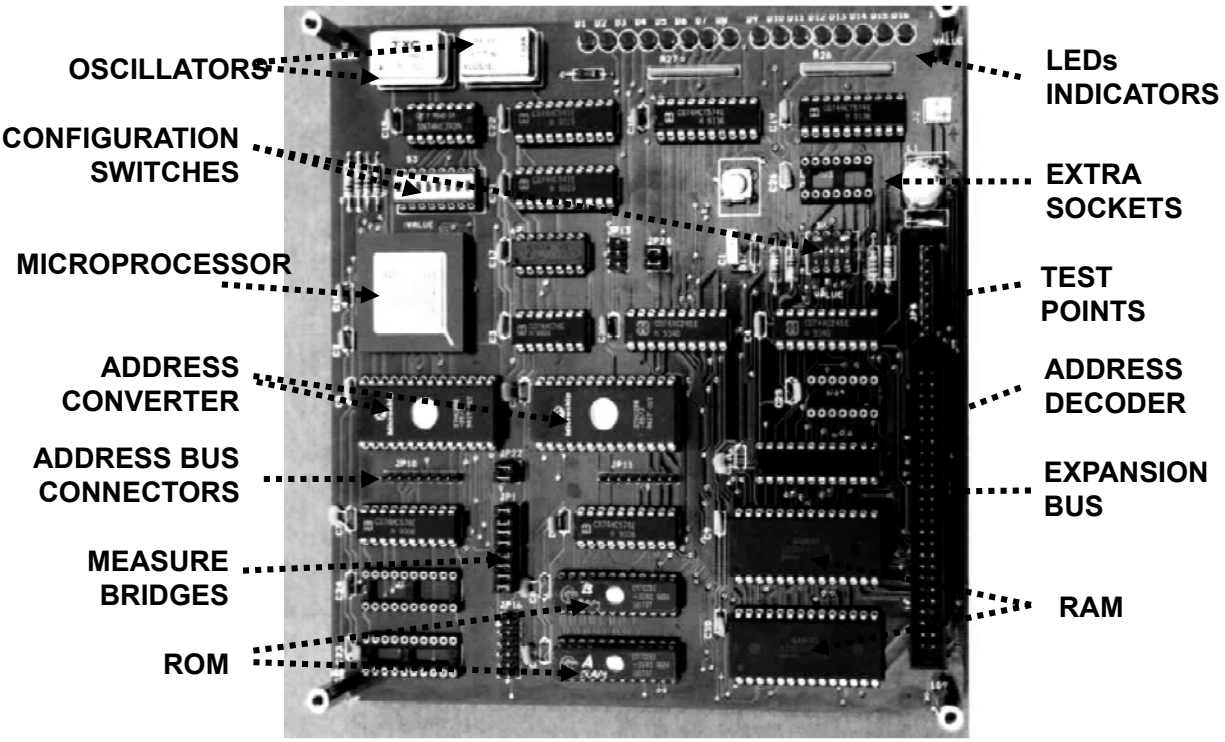


Five independent power supply lines:

a) the microprocessor
b) the 8KB ROM
c) the 8KB RAM
d) address converters
e) the miscellaneous logic.

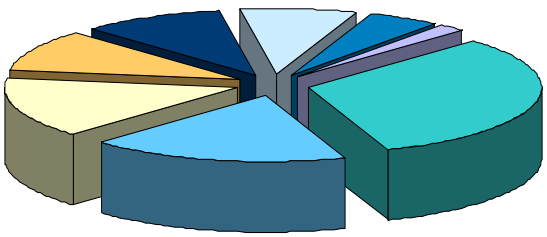
Different voltages can be applied to each block.

Power analysis and measurement at system level Example

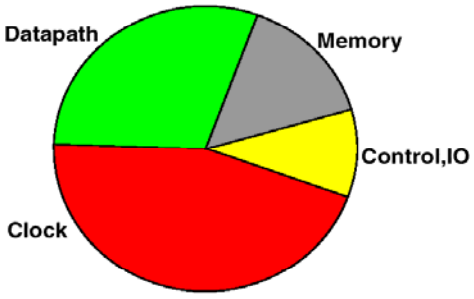


Source: G. Gonzalez de Rivera, J. Garrido, and E. Boemo, "Power Audit of an Space-Certified Microprocessor", *Proc PATMOS'99 (International Workshop Power and Timing Modeling, Optimization and Simulation)*, pp.551-556, October 6-8, Kos Island, Greece

Power analysis at chip level



- ← Alpha 21264. Source: [Gow98]



← Intel: Source: [Tiw98]

Power analysis at chip level

Static power	The chip is configured but neither stimulus nor clocking is applied. The pull-up resistors and other external elements that require the FPGAs remain connected.
Off-chip power	The circuit is measured twice. First, during normal operation. Second, by disabling the tri-state output buffers. Thus, the off-chip component can be approximated to the difference between the two results (In addition, the use of the tri-state buffers in low-power design is also useful to separate the results from a particular PCB).
Synchronization power	A constant data (for example, all bits zeroed) is inputted to the circuit, meanwhile the clock signal is applied. Thus, only the clock tree has activity. Is important to note that FPGAs use multiplexers to emulate the effect of a clock enable. As a consequence, the use of the *clock enable* pin of a CLB does not interrupt the clocking of the flip-flops.

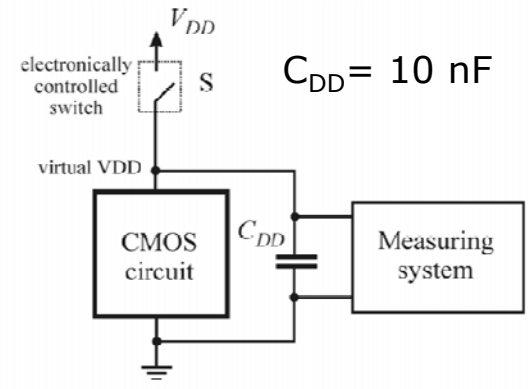
Source: E. Todorovich, G. Sutter, N. Acosta, E. Boemo and S. Lopez-Buedo, "End-user low-power alternatives at topological and physical levels. Some examples on FPGAs", *Proc. DCIS'2000 (XV Conference on Design of Circuits and Integrated Systems), pp.640-644, Montpellier, November 21-24, 2000*

Measuring power

- **Average power: Amperimeter**
  - The simple approach to measure *Icc is to connect* an ammeter in series with the supplying pins.
  - Periodic input pattern must be to the DUT. Thus, the resulting current waveform is periodic.
  - The ammeter averages the power supply current over a window of time and, if the period of the current waveform is much smaller than this window.

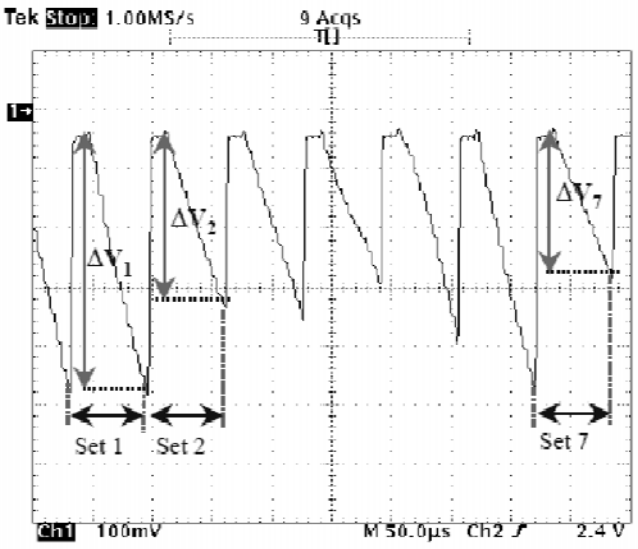
- **Dynamic Power (Method 1):**
  - Shunt Resistor + scope with differential probe
  - R between 2 and 100 Ω

Measuring clock-by-clock dynamic power



C_{DD}= 10 nF

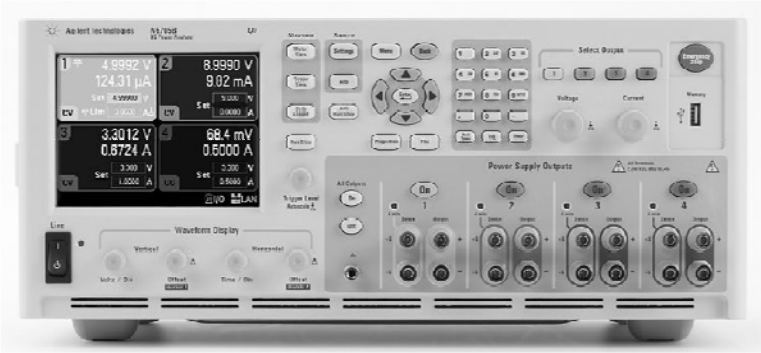
$$E=\frac{1}{2}C_{DD}V_{DD}^2-\frac{1}{2}C_{DD}\left(V_{DD}-\Delta V\right)^2=E_0\left[2\frac{\Delta V}{V_{DD}}-\left(\frac{\Delta V}{V_{DD}}\right)^2\right]$$



Source:

J. Rius-Vazquez, E. Boemo, A. Peidro Palanca, S. Manich-Bou and R. Rodriguez-Montañes, "Measuring Power and Energy of CMOS CIrcuits: A Comparative Analysis", Proceedings DCIS 2003 (XVIII Conference on Design of Circuits and Integrated Systems), pp. 89-94, Ciudad Real, November 2003.

Measuring power: Agilent N6705B DC Power Analyzer



- **4 power supply**
- **Voltmeter accuracy:** Up to 0.025% + 50 µV, up to 18 bits
- **Ammeter accuracy:** Up to 0.025% + 8 nA, up to 18 bits
- **Arbitrary waveform generator function:** Bandwidth up to 100 kHz, output power up to 300 W
- **Scope function:** Digitizes voltage and current at up to 200 kHz, up to 18 bits
- **Data logger function:** Measurement interval from 20 µs to 60 s.

A review of some LPD ideas to reduce Dynamic Power

$$P = \Sigma\, c\, f\, v^2$$

Dense LUT utilization:
- Σ (less nodes)
- c (less wires)
- f (less glitches)

Different topologies:
- Σ (different node count)
- c (different wire count
- c (different fanout)

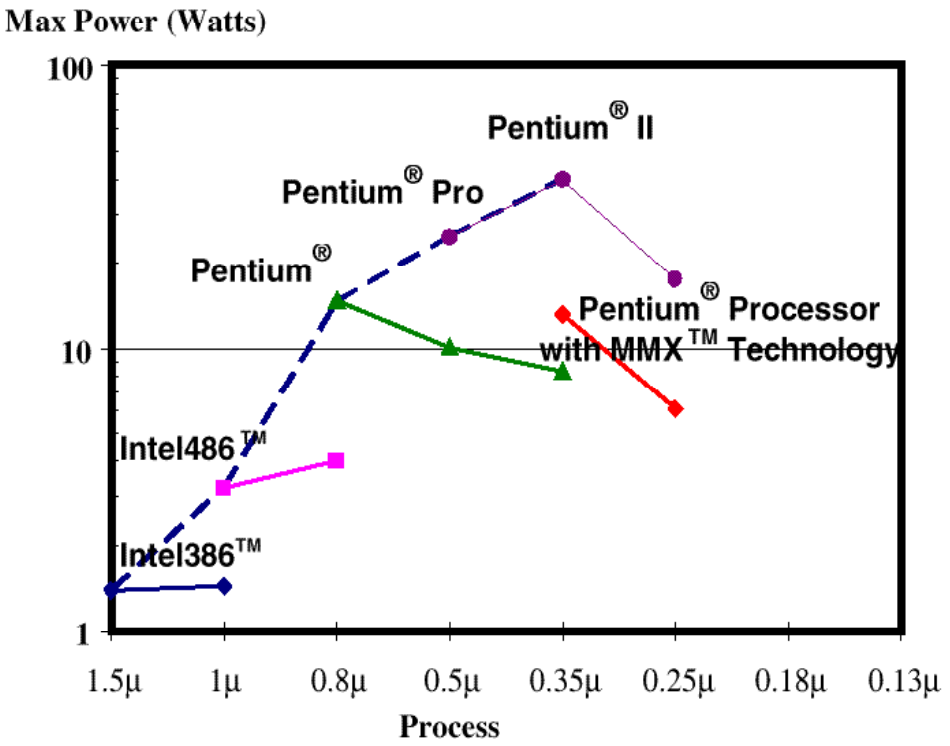
Manual Placement
- c (less wire length or capacitance)

Parallelism- Pipelining
- Σ (bigger node count)
- c (different wire count)
- c (different fanout)
- f (less glitches in pipelining)
- V (the lower can be selected)

Physical Design for high-speed
- c (different wire length)
- c (different fanout)
- V (the lower can be selected)

Clock gating /lowering clock
- f (less activity)

LPD Idea 1: Lowering scale integration Example: Intel



Source: Tiwari, 1998

LPD Idea 1: Lowering scale integration Example: Xilinx Spartan

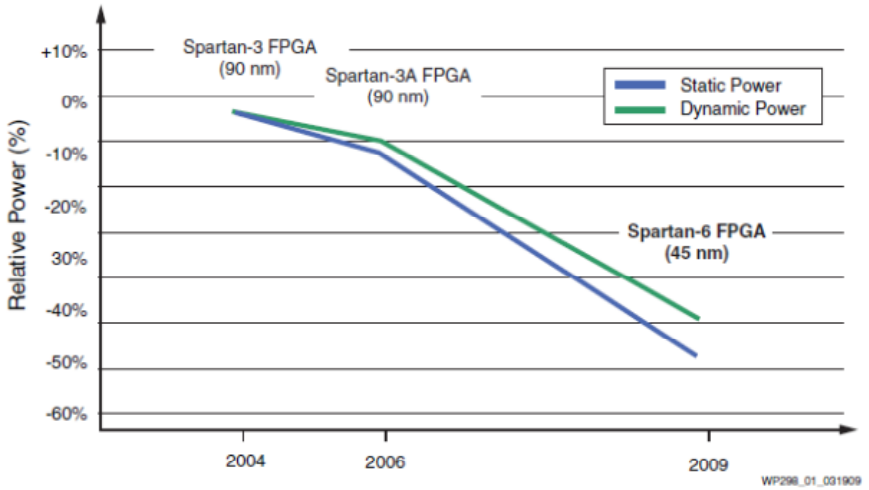


Figure 1: **Relative Power Consumption of Spartan-3A FPGAs**

- Discussion: Scaling change the components of the power. Example: short-circuit is 1-16% power at 0.7 micron, 4-37% at 0.35 micron, 12-60% at 0.17 micron

- **Source**: S. R. Vemuru and N. Steinberg, "Short Circuit Power Dissipation Estimation for CMOS Logic Gates," *IEEE Trans. on Circuits and Systems I*, vol. 41, Nov. 1994, pp. 762-765.

LPD Idea 2: Lowering Power Supply (Xilinx)

Table 2: **Virtex-5 FPGA Variation of Static and Dynamic Power Due to V_{CCINT} Core Voltage Adjustment**

V_{CCINT} Adjustments			Power Consumption from V_{CCINT}	
Voltage at FPGA	A%	mV	% Static	% Dynamic
0.95	-5	-50	-14.3	-9.8
0.96	-4	-40	-11.5	-7.8
0.97	-3	-30	-8.7	-5.9
0.98	-2	-20	-5.9	-4.0
0.99	-1	-10	-3.0	-2.0
1.00	0	0	0.0	0.0
1.01	1	10	3.0	2.0
1.02	2	20	6.1	4.0
1.03	3	30	9.3	6.1
1.04	4	40	12.5	8.2
1.05	5	50	15.8	10.3

Notes:
1. All variations are shown relative to the highlighted Virtex-5 FPGA nominal V_{CCINT} of 1V.

***Source**: P. Abusaidi, M. Klein, and B. Philofsky, **Virtex-5 FPGA System Power Design Considerations**,* Xilinx Inc. 2008

- *"… Since the Virtex-5 FPGA can operate within its specifications even with a voltage of 0.95V, some power benefit can be achieved by adjusting VCCINT to slightly below the nominal voltage, such as 0.98V".*

- *P static ~ kV^3*

- *ΔV acceptable = ± 5%*

LPD Idea 3: Low-voltage FPGAs

As shown in Equation 1, dynamic power is proportional to the square of input voltage. Static power is approximately proportional to the cube of input voltage. Obviously, reducing core voltage offers large power savings.

To realize these savings, Xilinx has created voltage-scaled versions (-1L) of devices in the Spartan-6 and Virtex-6 FPGA families. Essentially, the devices are the same—but with core voltage scaled from 1.2V to 1V in Spartan-6 devices and from 1V to 0.9V in Virtex-6 devices.

As predicted by the equations for dynamic and static power, and illustrated in Table 7, the power savings are large. Spartan-6 FPGA core power is lowered an additional 30–40% on top and independent of savings from process and architecture, and Virtex-6 FPGA core power is lowered an additional 20–25%.

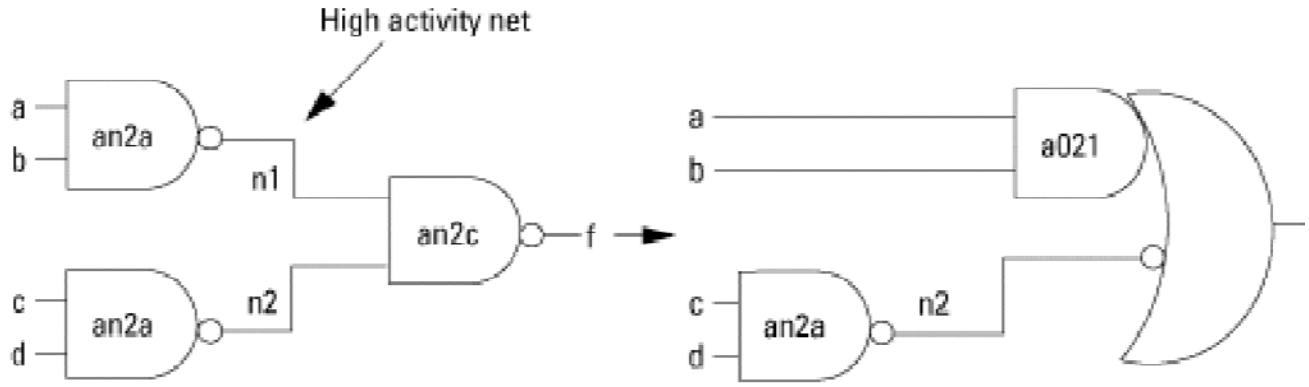
Table 7: **Power Savings of -1L Devices over Standard Voltage Devices**

	Spartan-6 FPGA		Virtex-6 FPGA	
	Standard	-1L	Standard	-1L
V_{CCINT}	1.2V	1V	1V	0.9V
Static Power	Nominal	–42%	Nominal	–26%
Dynamic Power	Nominal	–31%	Nominal	–20%

- Drawback: $t_D = \frac{C_L}{I_{AVE}} \times \frac{V_{DD}}{2} \cong \frac{C_L \times V_{DD}}{k_P \times (V_{DD} - V_T)^2}$

LPD Idea 5: Use of equivalent hardwired cells (AOI, OAI, …)

Target: Glitch reduction



$$Pow(n1) = TR_{n1} \times Cap_{n1} \times V^2/2$$

Source: Synopsys

LPD Idea 5 (in FPGA): Use of equivalent hard-macros

Up to 90% reduction in static power compared to soft-IP implementations.	Selecting a set of common blocks needed by many customers allows Xilinx to offer better performance and lower static and dynamic power.

Xilinx has a long history of having a rich set of integrated blocks (e.g., Ethernet MAC, DSP, and PCIe® blocks). This generation of devices now has even more hard blocks, especially in the Spartan-6 family (e.g., PCIe block, hard memory controller, and enhanced DSP). Use of these blocks reduces static and dynamic power and frees up logic for user designs.

- Discussion: What can be deduced from this Xilinx text?

Answer: The extra power of FPGA respect to CBIC can be nearly a 10x factor.

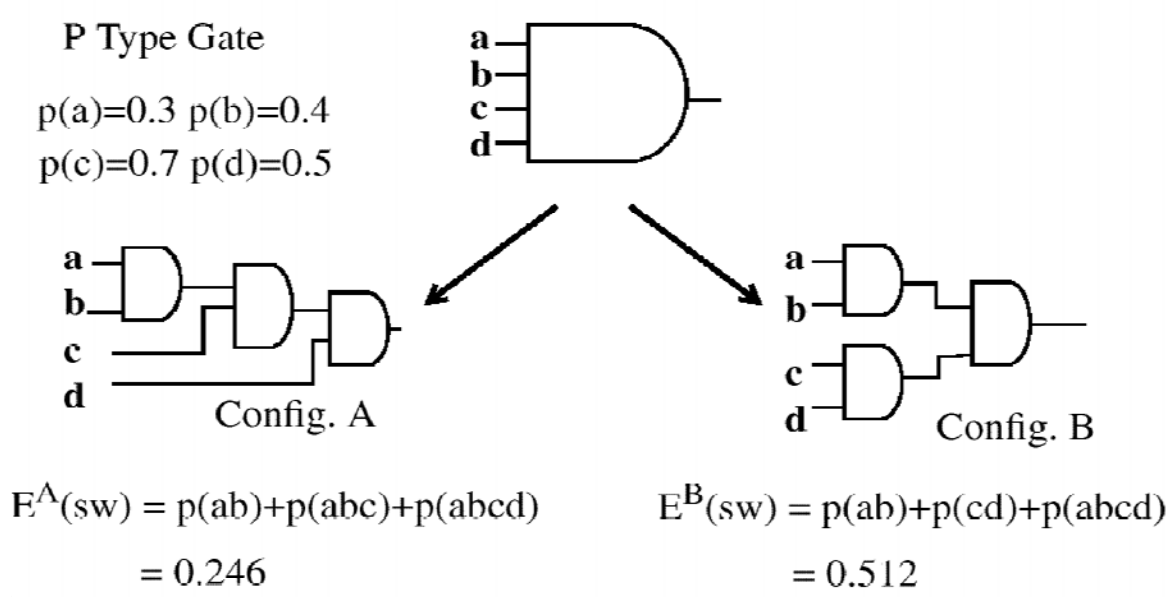
LPD Idea 6: Dense utilization of LUTs

Table 5: **Resource Use Reduction Using LUT6 Architecture for LUT6-Based Design**

Telecom Design	LUTs	Nets	Connections	Routing Resources
LUT4	18,371	26,417	100,641	95,200
LUT6	14,585	22,510	89,569	82,408
% Reduction	–21%	–14.8%	–11%	–13.5%

- Manual partitioning or dense occupation(CLBMAP, FMAP, HMAP, LOC, etc.) is also effective.
  - # LUTs ↓
  - Logic depth ↓
  - # Nodes ↓
  - Wiring delay ↑
  - But … P ↓

LPD Idea 7: Reordering of high activity signals



Source: Pedram (USC)

Idea: The faster signal as near the output as possible

LPD Idea 8: Special Place&Route of high activity nodes

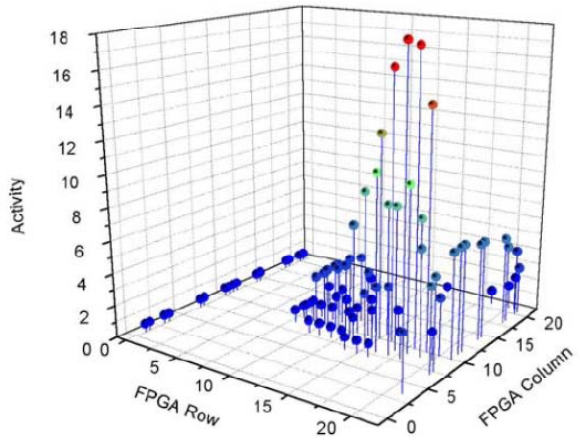
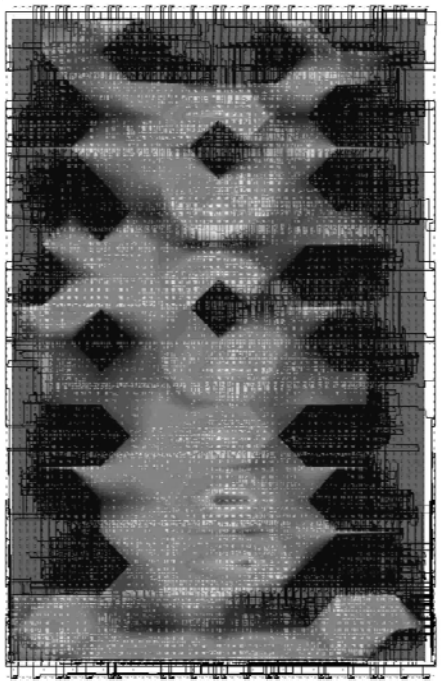


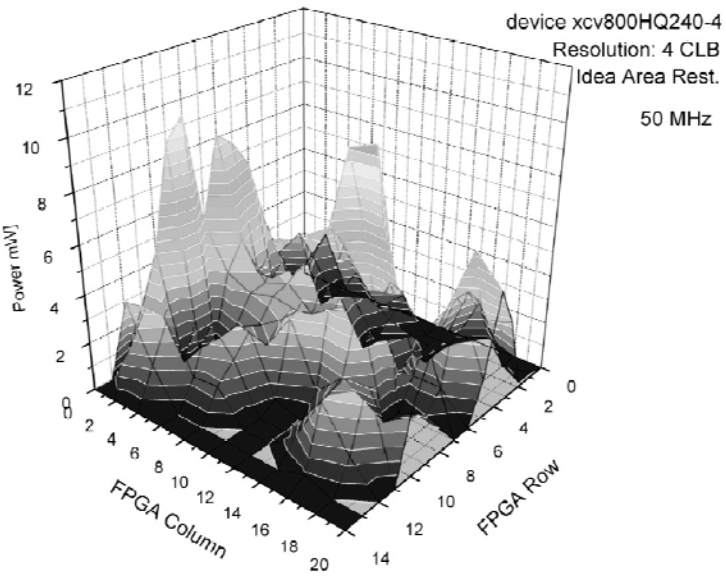
Fig. 1. 8-bit multiplier activity over a 20 × 20 CLB XC4010E FPGA. Node activities belonging to a single CLB are added

- **Source:**
- E. Todorovich, E. Boemo, F. Angarita, and J. Valls, "Statistical power estimation for FPGAs", *FPL 2005 (XV International Conference on Field Programmable Logic and Applications)*, pp.515 - 518, Tampere, Finland, August 2005. IEEE Press. ISBN: 0-7803-9362-7

- **Idea**: To minimize wire capacitance of high-activity nodes
- **Actions**:
  - Simulation to detect the candidate nodes.
  - *Floorplanning.*
  - PPR manual (Xilinx)
  - Time specification to the automatic PPR

LPD Idea 8: Special Place&Route of high activity nodes





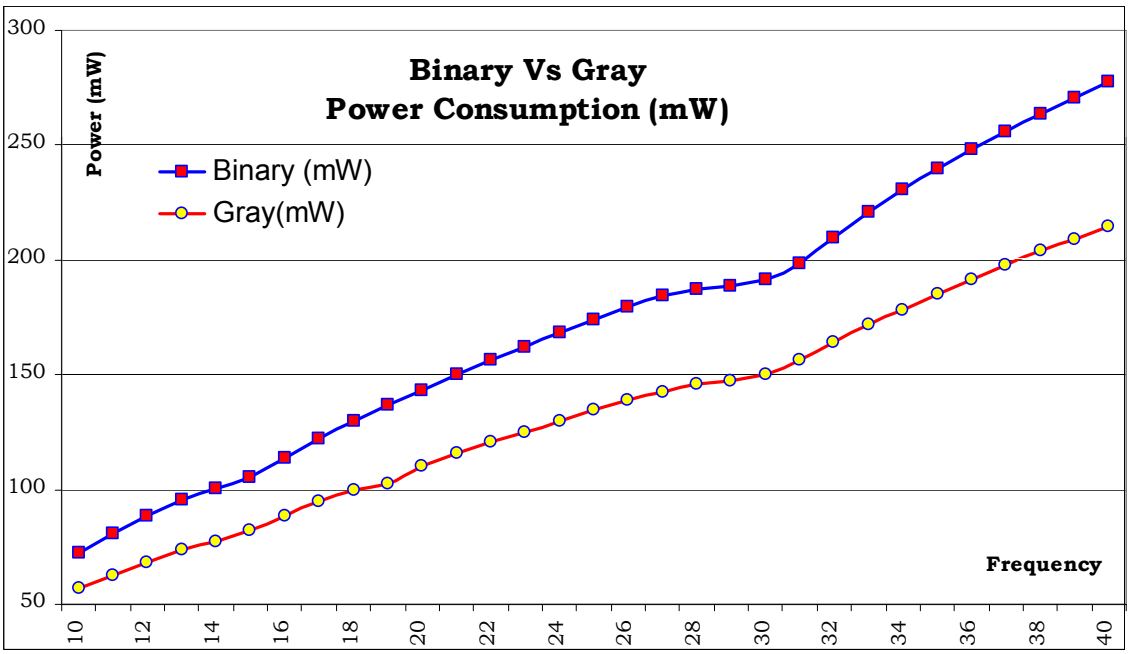
- **Source**: Elias Todorovich PhD Thesis , UAM 2006

LPD Idea 9: Bus/State Coding

State	One Hot	Gray	Binary
S0	00000001	000	000
S1	00000010	001	001
S2	00000100	011	010
S3	00001000	010	011
S4	00010000	110	100
S5	00100000	111	101
S6	01000000	101	110
S7	10000000	100	111
Total Number of Transitions	16	8	11
Maximum Transitions Per Clock Cycle	2	1	3
Clock Load	8	3	3

Source: Jonathan Alexande, Actel Corporation

LPD Idea 9: Bus/State Coding

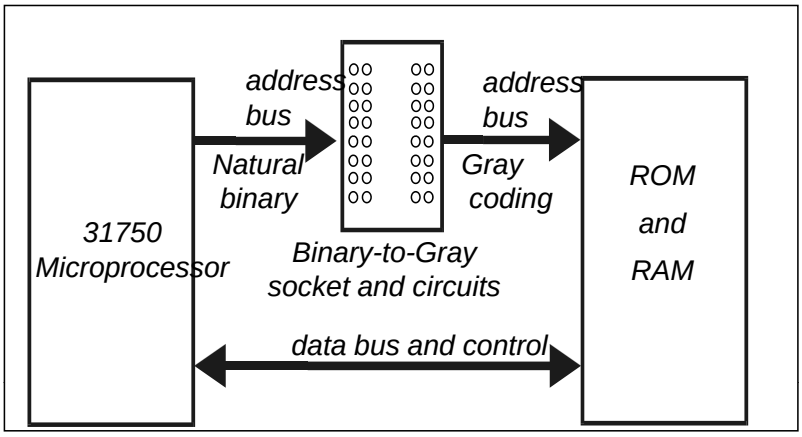


Source: Jonathan Alexande, Actel Corporation

- Consumo de 200 instancias: Contador binarios vs. Gray

LPD Idea 9: Bus/State Coding
Gray Coding – Bus Invert

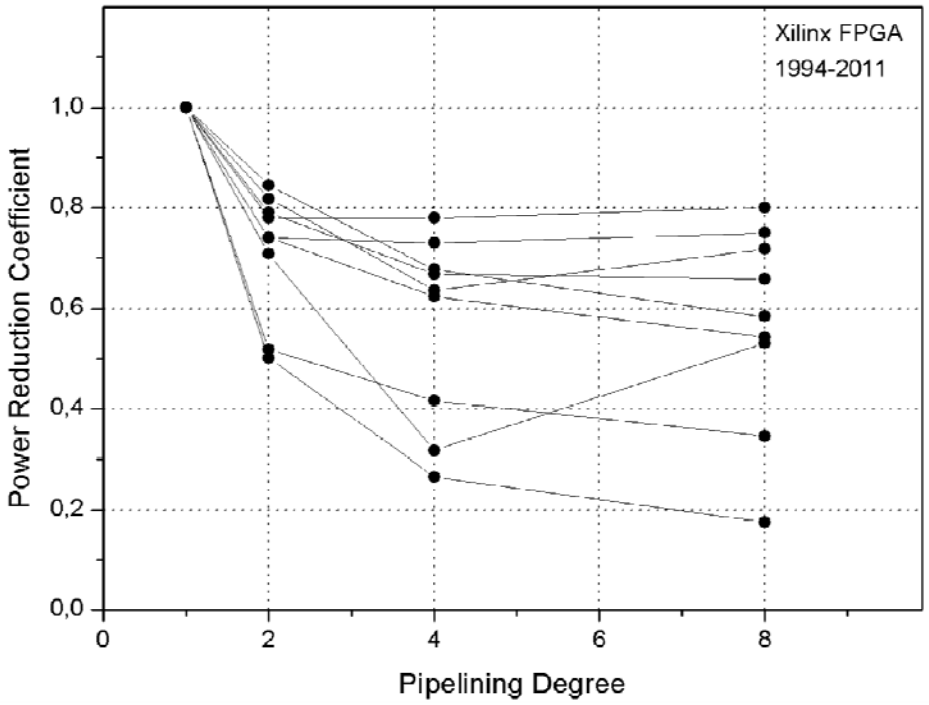
The processor accesses to the instructions sequentially most of the time.



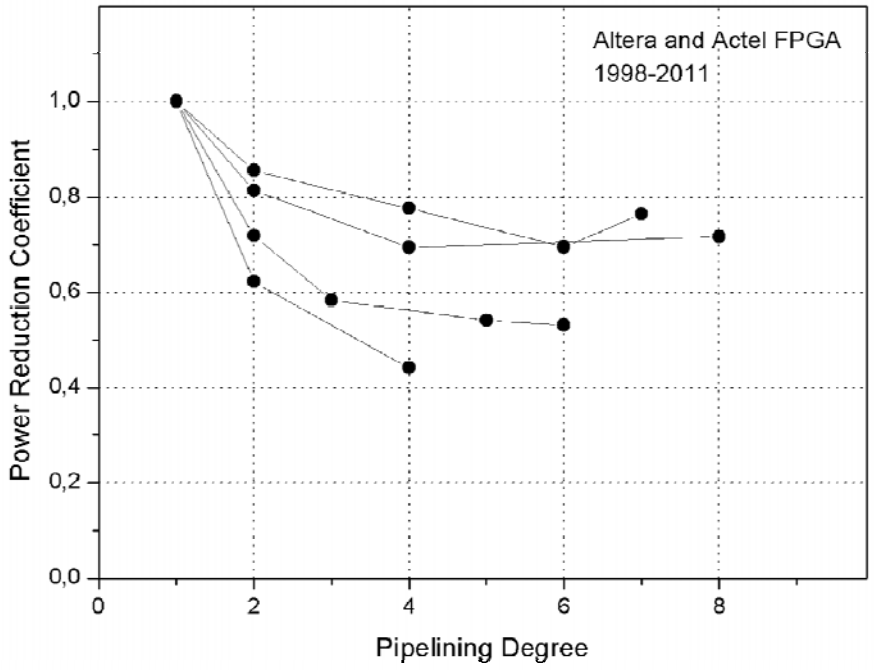
For the experiment, we needed:

- To convert natural to Gray code: EPROM (look-up table), PAL or discrete.
- To allocate the program's instructions in a Gray sequence.

LPD Idea 10: Glitch reduction by pipelining Example Xilinx

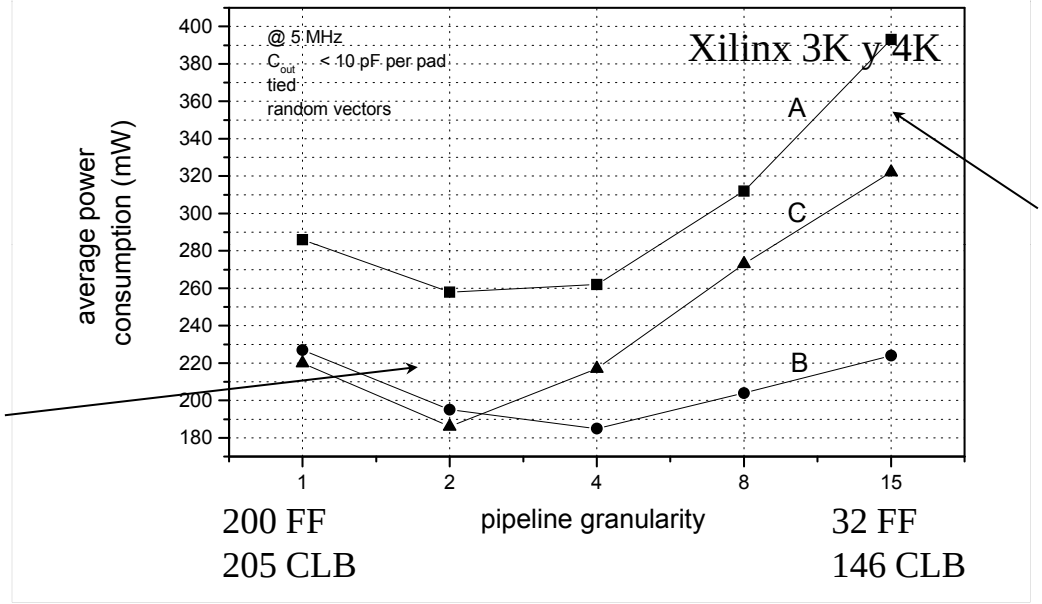


LPD Idea 10: Glitch reduction by pipelining Example Actel and Altera



LPD Idea 10: Glitch reduction by pipelining

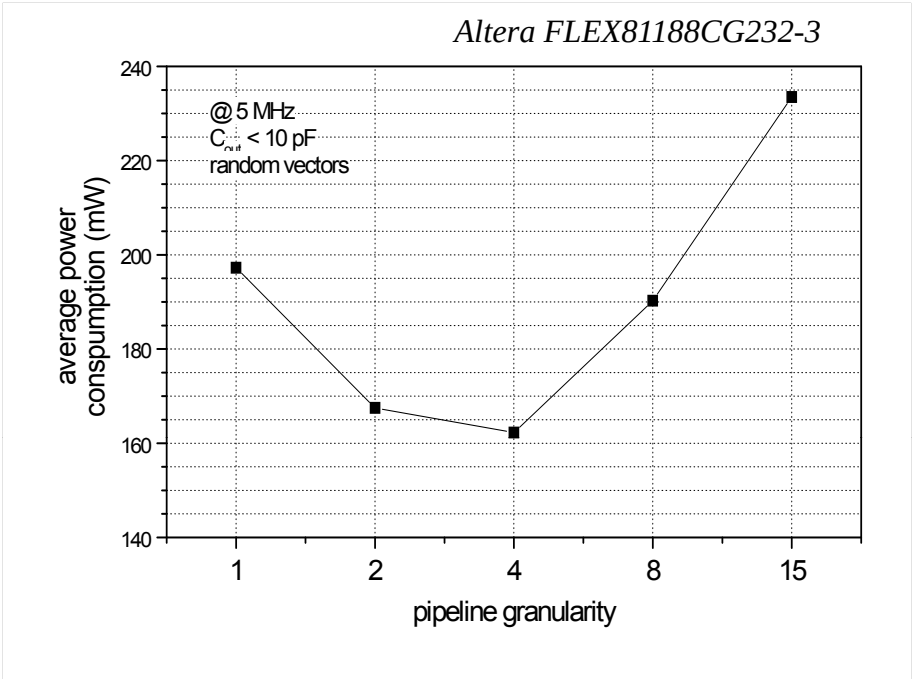
Source. E. Boemo, PhD Thesis, 1996



- A: XC3090, *default* PPR.
- B: XC3090, manual partitioning en LUTs.
- C: XC4005, *default* PPR

LPD Idea 10: Glitch reduction by pipelining

Source. E. Boemo, PhD Thesis, 1996



Moderate pipelining reduce significantly the power in all FPGAs

10 years

3 series

3 manufacturers.

LPD Idea 10: Glitch reduction by pipelining Area Penalty

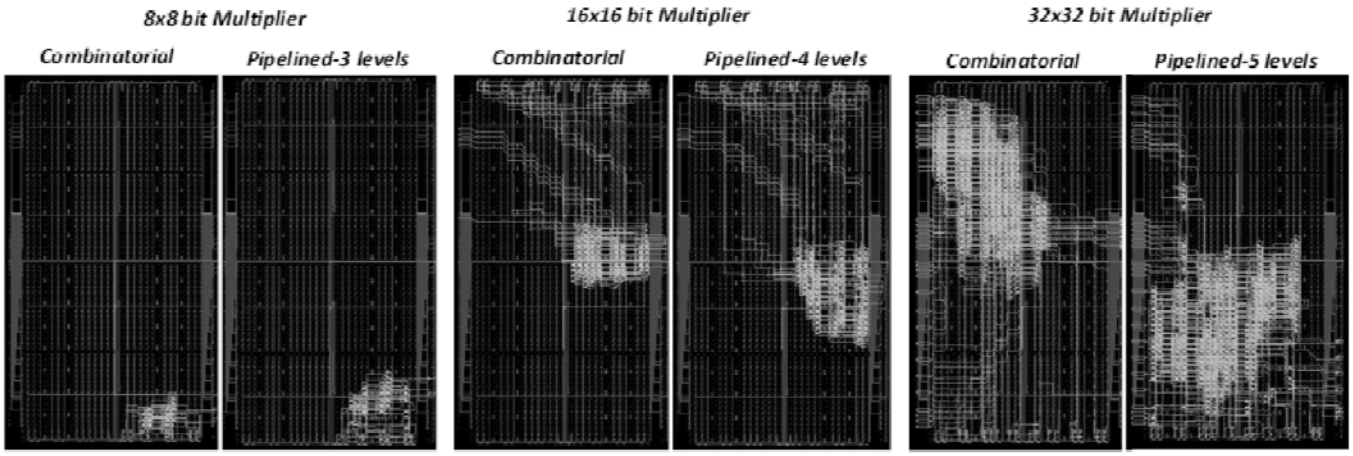
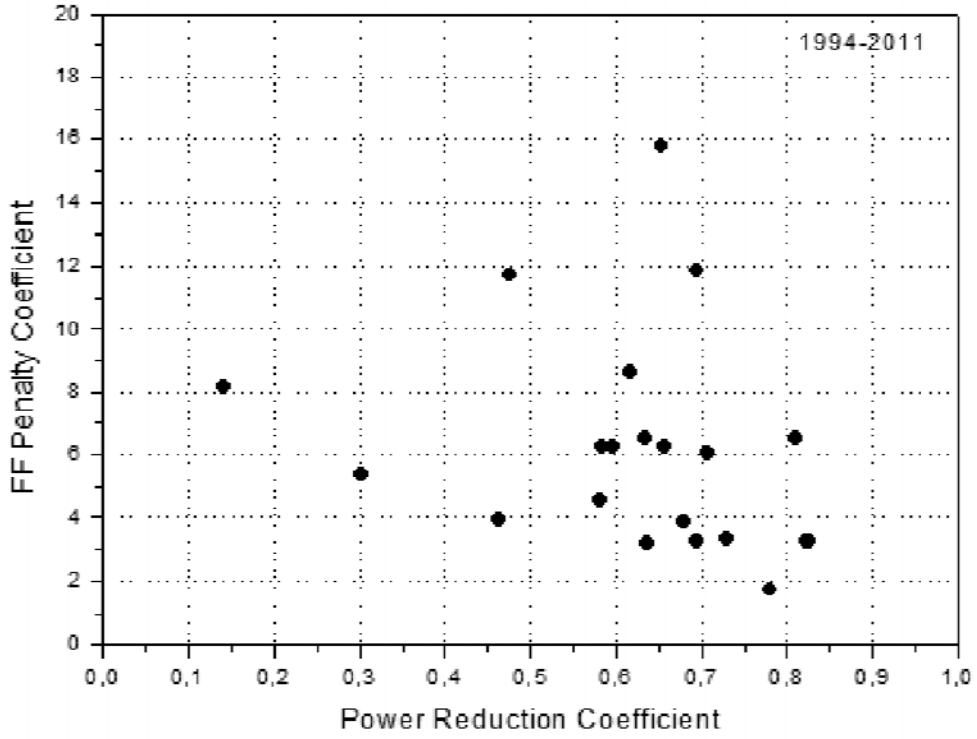


Figure 2.23 Area growth vs. bit size and vs. various segmentation levels.

Alex Caraba, "Analysis of FPGA – programmable devices in 0.45 nm technology" Master Thesis – UAM, 2011

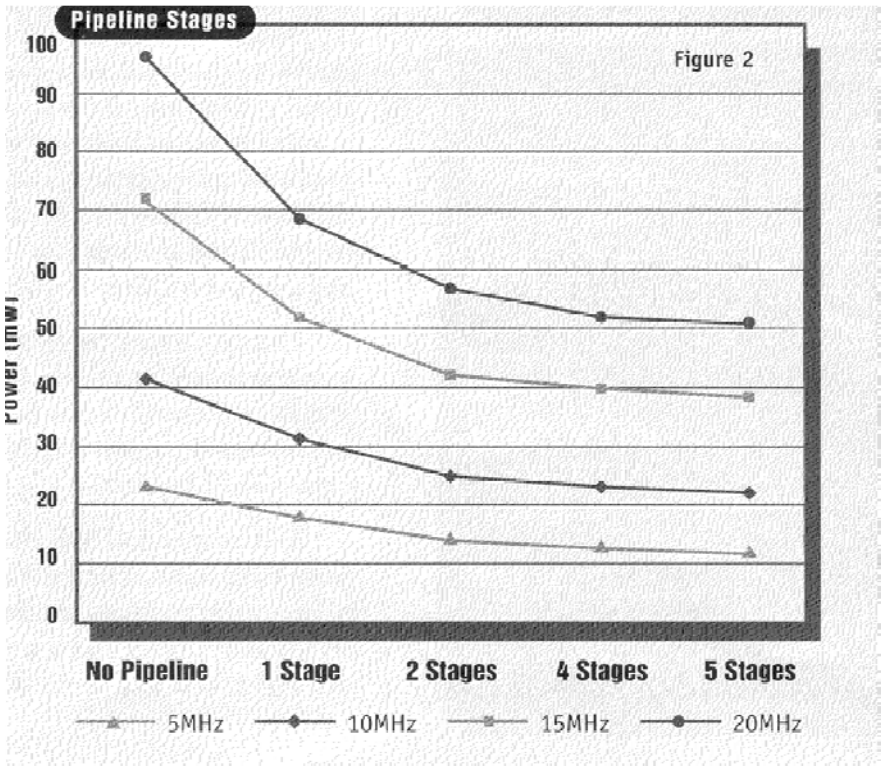
LPD Idea 10: Glitch reduction by pipelining Area Penalty



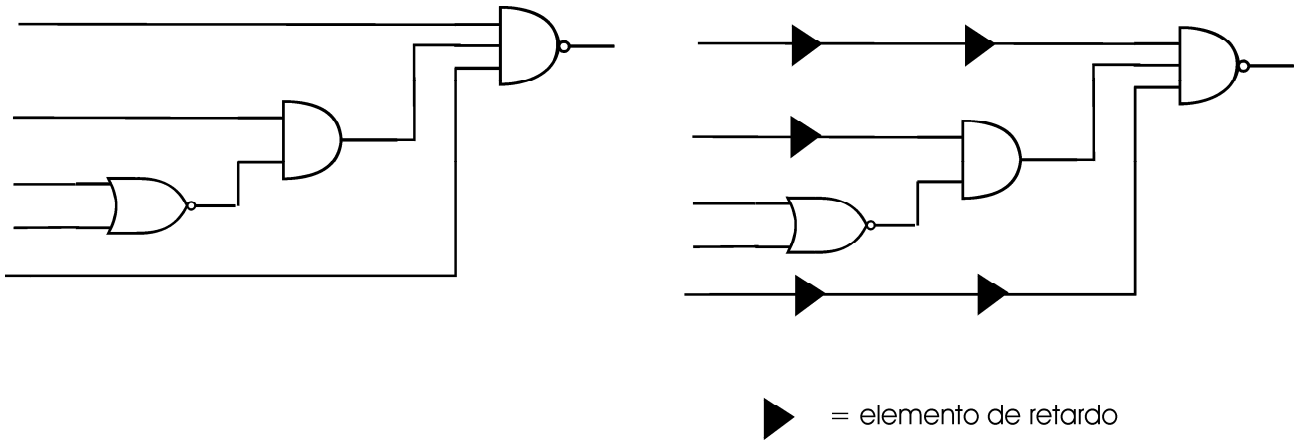
LPD Idea 10: Glitch reduction by pipelining Conclusions

- **Power reduction up to:**
  - **- 33 % (XC3090)**
  - **- 58 % (XC4005)**
  - **- 85 % (Virtex)**
  - **- 30 % (Altera Flex)**
- **Cost:**
  - **Number of registers**
  - **Latency**
- ***Manual partitioning*** **(CLBMAP, FMAP, HMAP, LOC, etc.) is also effective.**
  - ***LUTs*** ↓
  - ***Logic depth*** ↓
  - ***Nodes*** ↓
  - ***Wiring delay*** ↑
  - ***But … P*** ↓

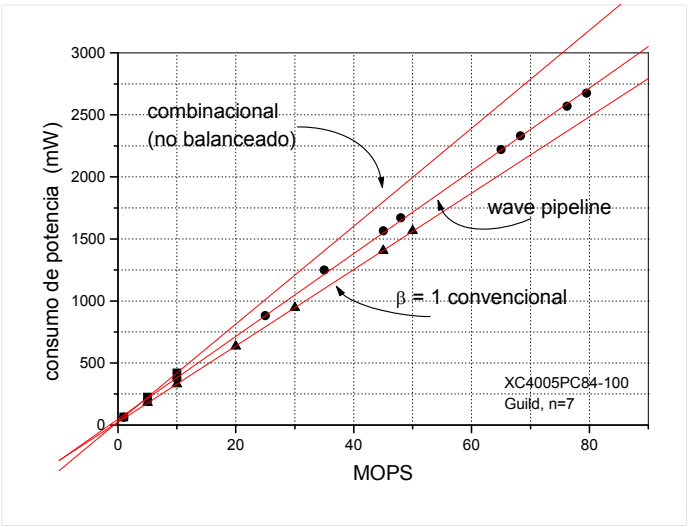
LPD Idea 10: Pipelining as LPD Technique (Actel)

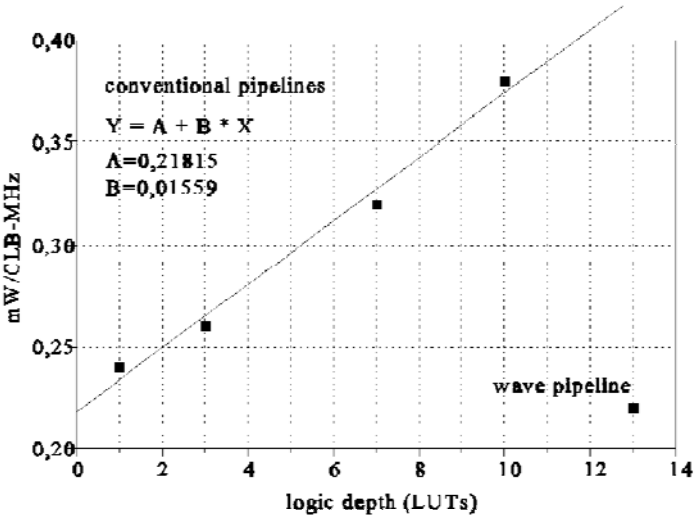


LPD Idea 11: Path equalization to reduce glitches → WP (Wave Pipeline)



LPD Idea 11: Path equalization to reduce glitches → WP (Wave Pipeline)

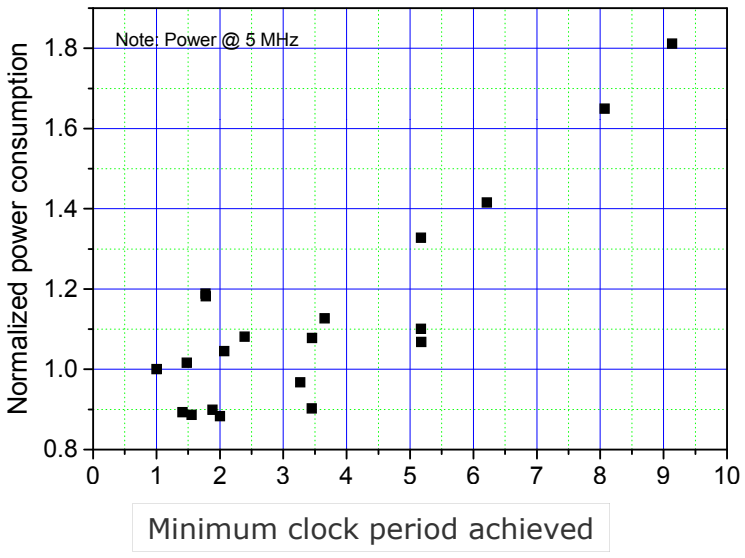




E. Boemo, S. Lopez-Buedo, and J. Meneses, "Some Experiments about Wave Pipelining on FPGAs", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.6, No.2, June 1998.

WP doesn't work as LPD strategy.

LPD Idea 12: More BW - Less Power

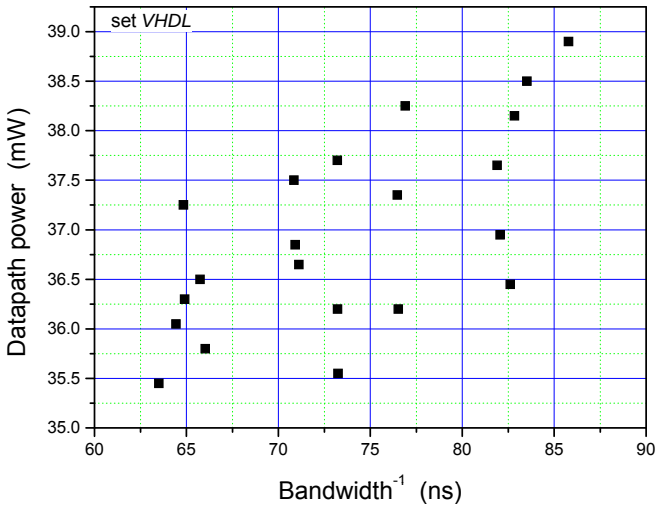


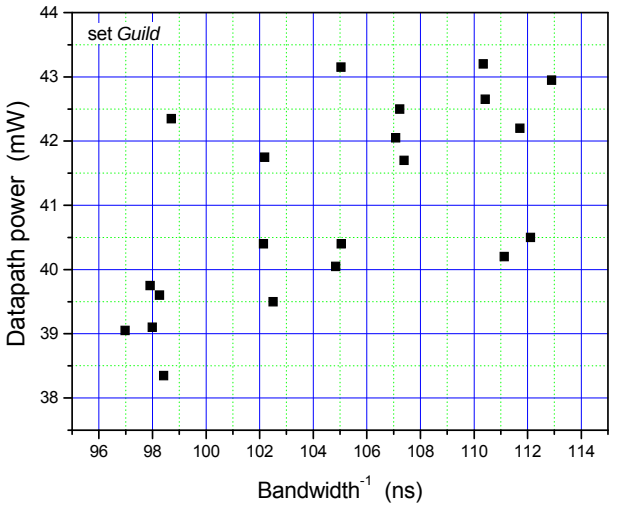
- Peter Alfke idea: more speed need lower wire capacitances, and lower wire capacitances lead to less power

← Power versus minimun clock period reachable of identical multipliers with different PPRs

- **Source**: *"Contribución al Diseño de Arrays VLSI",* E. Boemo, UPM: 1995.

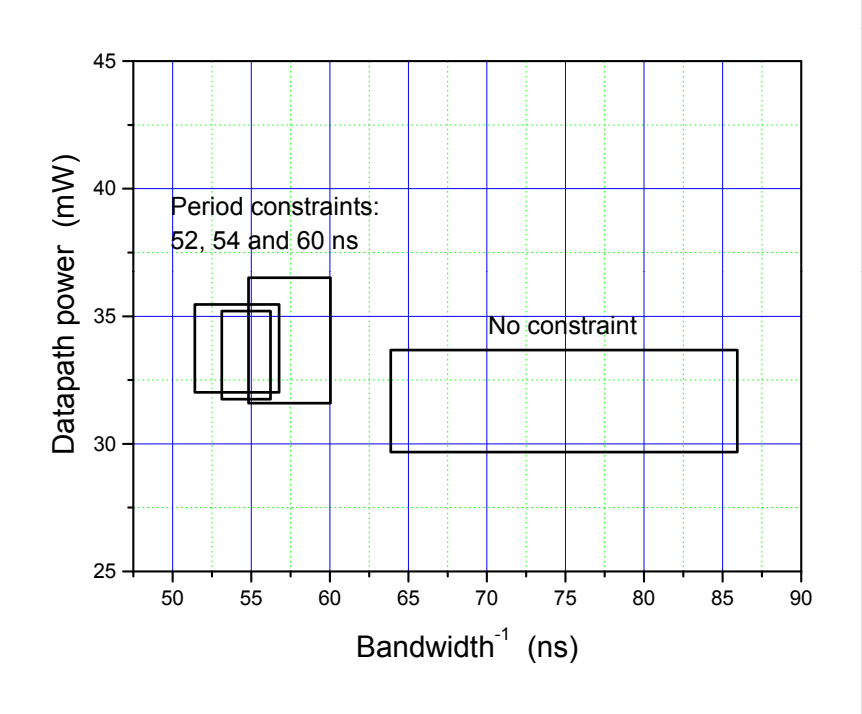
LPD Idea 12: More BW - Less Power





It can be stated as a rule of thumb, that circuits than run faster, use less CLBs and dissipate less power. The common origin of these improvements is the reduction of the interconnection capacitance.

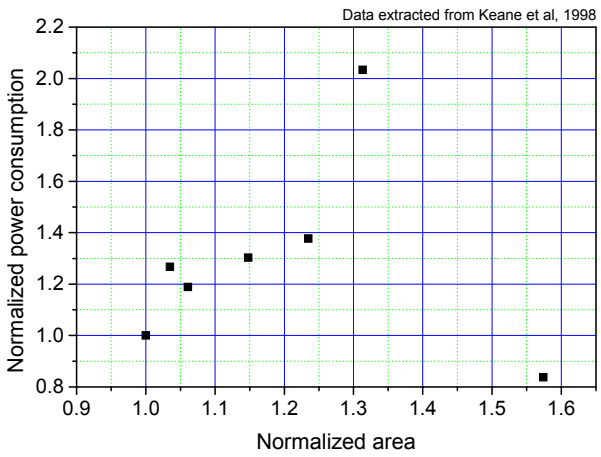
LPD Idea 12: More BW - Less Power
Forcing the idea

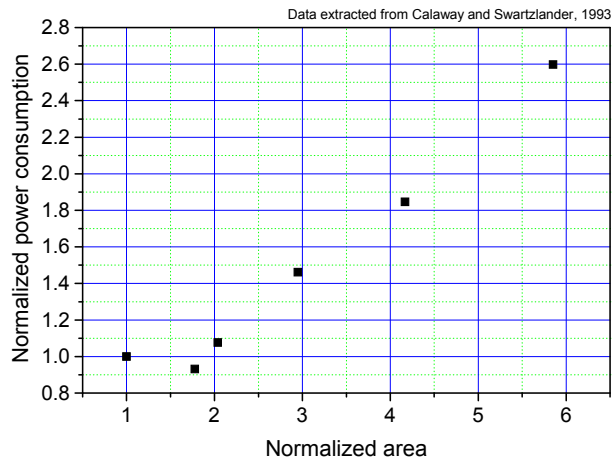


Timing constraint doesn't work as LPD strategy

E. Todorovich, G. Sutter, N. Acosta, E. Boemo and S. Lopez-Buedo, "End-user low-power alternatives at topological and physical levels. Some examples on FPGAs", *Proc. DCIS'2000 (XV Conference on Design of Circuits and Integrated Systems), pp.640-644, Montpellier, November 21-24, 2000.*

LPD Idea 13: Less Area - Less Power



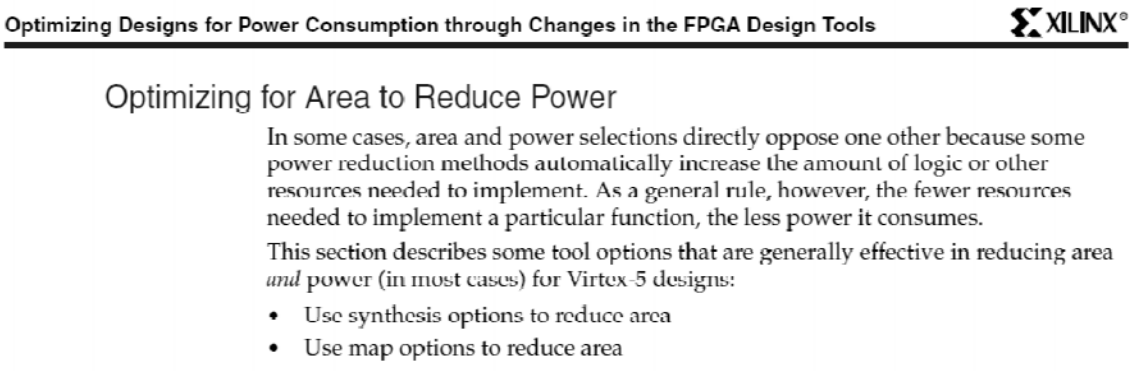


LPD Idea 13: Less Area - Less Power
Use of tool to minimize area and indirectly power

13 years between Academic and Industry!

• EIB 1995: *"Contribution of fine-grain pipelined arrays",* Ph.D. Thesis, ETSI UPM Dec 1995.

• Xilinx Inc: WP285 (v1.0) February 14, 2008.



Optimizing Designs for Power Consumption through Changes in the FPGA Design Tools XILINX®

Optimizing for Area to Reduce Power

In some cases, area and power selections directly oppose one other because some power reduction methods automatically increase the amount of logic or other resources needed to implement. As a general rule, however, the fewer resources needed to implement a particular function, the less power it consumes.

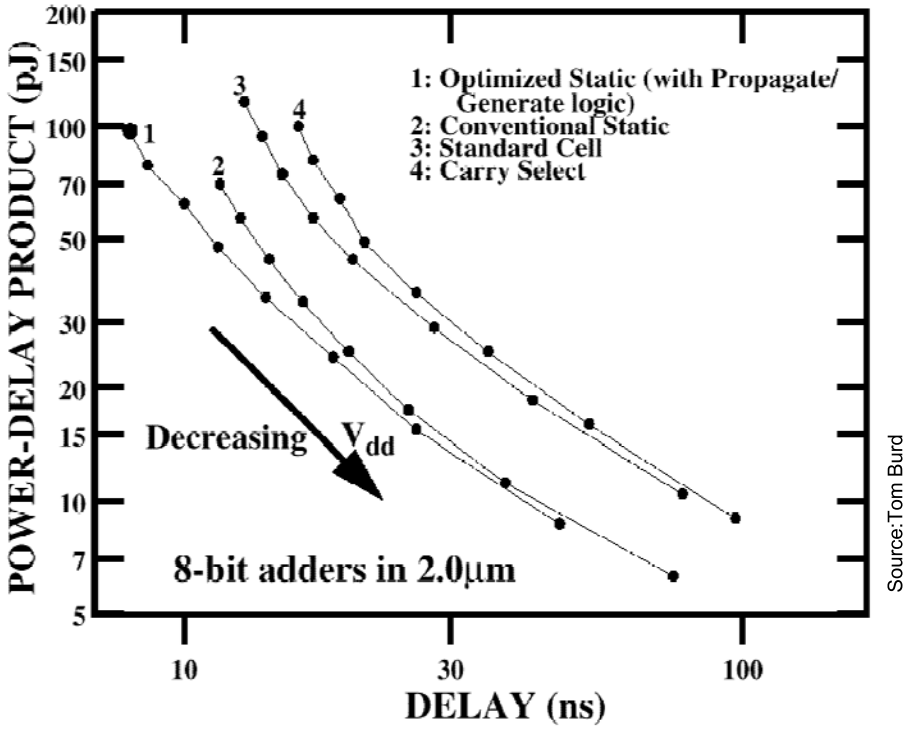
This section describes some tool options that are generally effective in reducing area *and* power (in most cases) for Virtex-5 designs:

- Use synthesis options to reduce area
- Use map options to reduce area

LPD Idea 14: Topology vs. Area-time-power

- Most of the custom DSP need Multipliers-Adders
  - ¿How many form of multipliying exist? ? (*Guild, Hatamian, CSA, Booth, Wallace, etc*).
  - ¿And how many adders? (*ripple-carry, carry-save, carry-skip, carry look-ahead, Brent & Kung, Khün, etc.)*
- Different operators can be selected from VHDL, libraries, synthesis options, etc. Each one will have an unique ATP diferente.
- Topologies can be combined then with pipelining, digit-serial, parallelism, etc .

LPD Idea 14: Topology vs. Area-time-power



Source:Tom Burd

LPD Idea 14: Topology vs. Area-time-power Mentor results

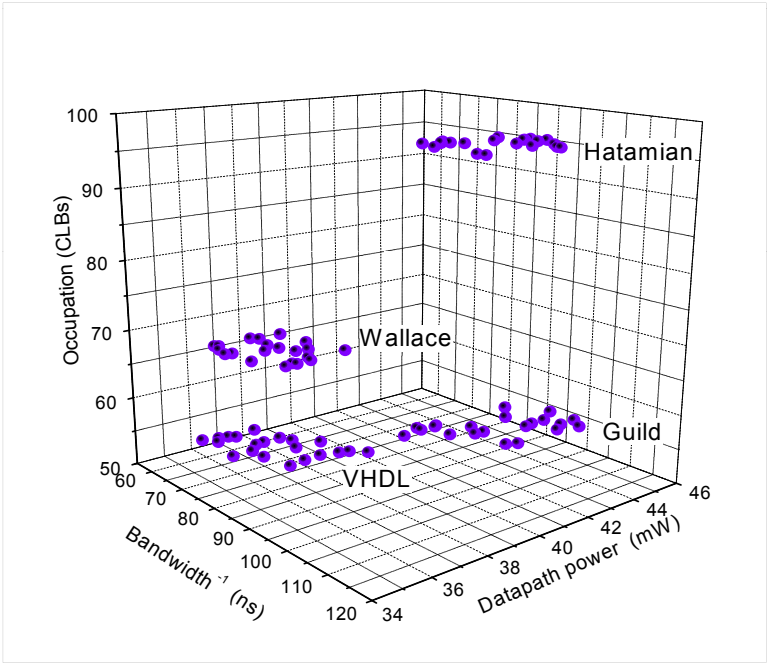
Mentor Graphics, 2006:
Same filter response but different implementations

Project Files | XY Plot | Bar Chart | Table

Solution	Status	Total Area Score	Latency Cycles	Latency Time	Throughput Cycles	Throughput Time	Power Consumption
DIRECT_FORM	Passed extract	5140.63	18	45.00	18	45.00	2.66 mW
DIRECT_FORM_THRUPUT_1	Passed extract	30212.40	1	2.50	1	2.50	6.66 mW
DIRECT_FORM_AREA_OPT	Passed extract	4040.64	18	45.00	16	40.00	2.68 mW
REG_ROTATE	Passed extract	6685.45	63	157.50	63	157.50	2.56 mW
REG_ROTATE_LP	Passed extract	4822.77	56	140.00	56	140.00	2.03 mW
REG_ROTATE_AREA_OPT	Passed extract	3368.06	8	20.00	8	20.00	3.03 mW
REG_ROTATE_PARTIAL	Passed extract	6201.16	4	10.00	4	10.00	3.71 mW

Figure 5: Power consumption for different implementations of a FIR filter algorithm

LPD Idea 14: Topology vs. Area-time-power



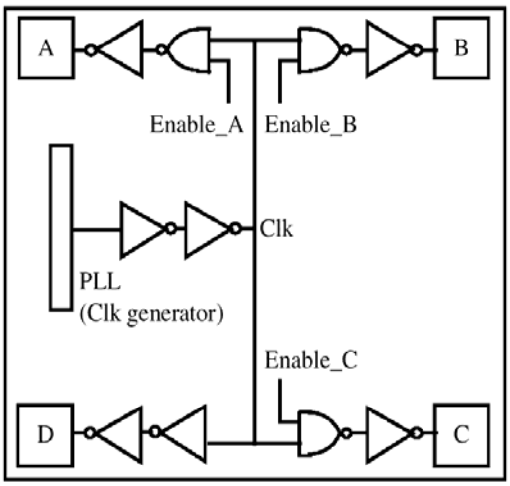
- For a selected topology, maximum bandwidth usually points to the best circuit in terms of power.
- If the designer must choice between different topologies, neither clock period nor occupation are primary parameters by themselves to predict a power saving.

E. Todorovich, G. Sutter, N. Acosta, E. Boemo and S. Lopez-Buedo, "End-user low-power alternatives at topological and physical levels. Some examples on FPGAs", *Proc. DCIS'2000 (XV Conference on Design of Circuits and Integrated Systems), pp.640-644, Montpellier, November 21-24, 2000.*

LPD Idea 15: *Clock Gating*

OP	1011011	address or data

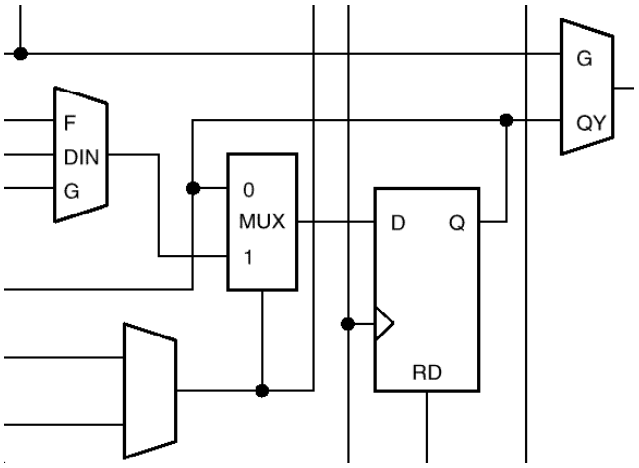
- **Example µP:**
- The instruction include the disable bits of the blocks that do not participate in the instruction.
- **Problems:**
  - Wake-up.
  - *Glitches in the clock tree*.
  - Extra *skew*.
  - Placement.

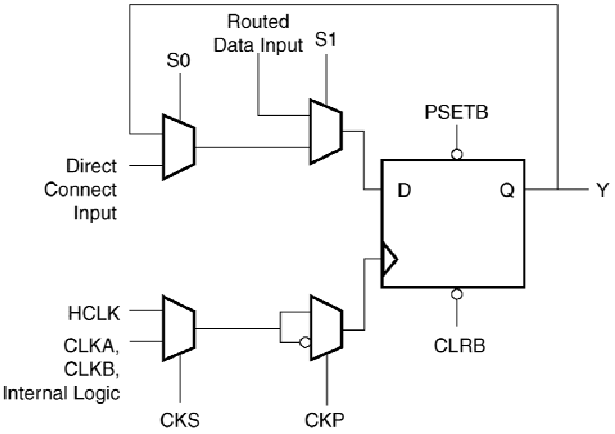


Source: [Tiw98]

LPD Idea 15: Clock Gating
Be careful in some FPGAs

- In some FPGAs the *clock enable* has not effect on synchronization power (clock tree power)





- Ejxamples: CE mechanisms in Xilinx XC3K and Actel SX

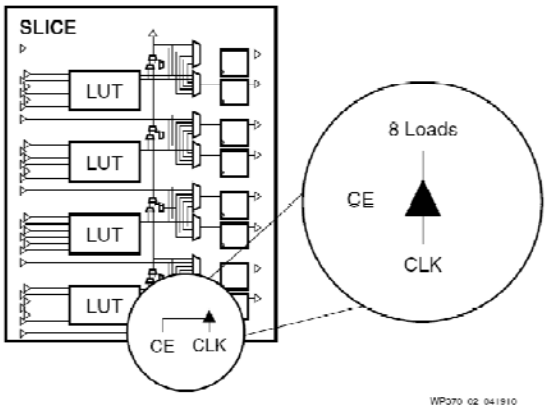
LPD Idea 15: Clock Gating
Xilinx actions in Clock Gating

"… perform an analysis on all portions of the design (including legacy and third-party IP blocks).

"… detect sourcing registers that do not contribute to the result for each clock cycle.

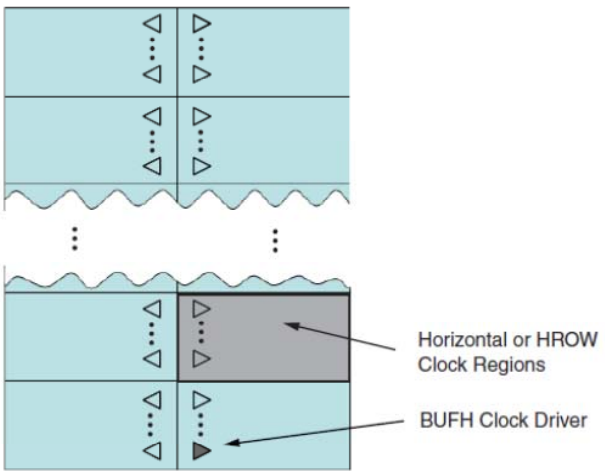
"… the software utilizes the abundant supply of clock enables (CEs) available in the logic to create fine-grain clock-gating or logic-gating signals"

- Spartan-6 FPGAs in ISE 12.3, and ISE 13.1 adds support for both Kintex-7 and Virtex-7 FPGAs.
- Cost: 2% extra LUTs.



Source: ***Reducing Switching Power with Intelligent Clock Gating,*** *Frederic Rivoallon, Xilinx Inc,* March 1, 2011

LPD Idea 15: Clock Gating
Xilinx actions in Clock Gating



- Logic mapped in a clock region, can be switch-off, disabling the corresponding BUFH.
- BUFH is the finest grain to control power
- Example:
  - A control FSM can have output bits to turn-on or turn-off part of the circuit.
  - A custom processor can include gate-clock bits in its instruction format

OP code	Gate clocking bits	Address or data

LPD Idea 15: Clock Gating
Xilinx actions in Clock Gating

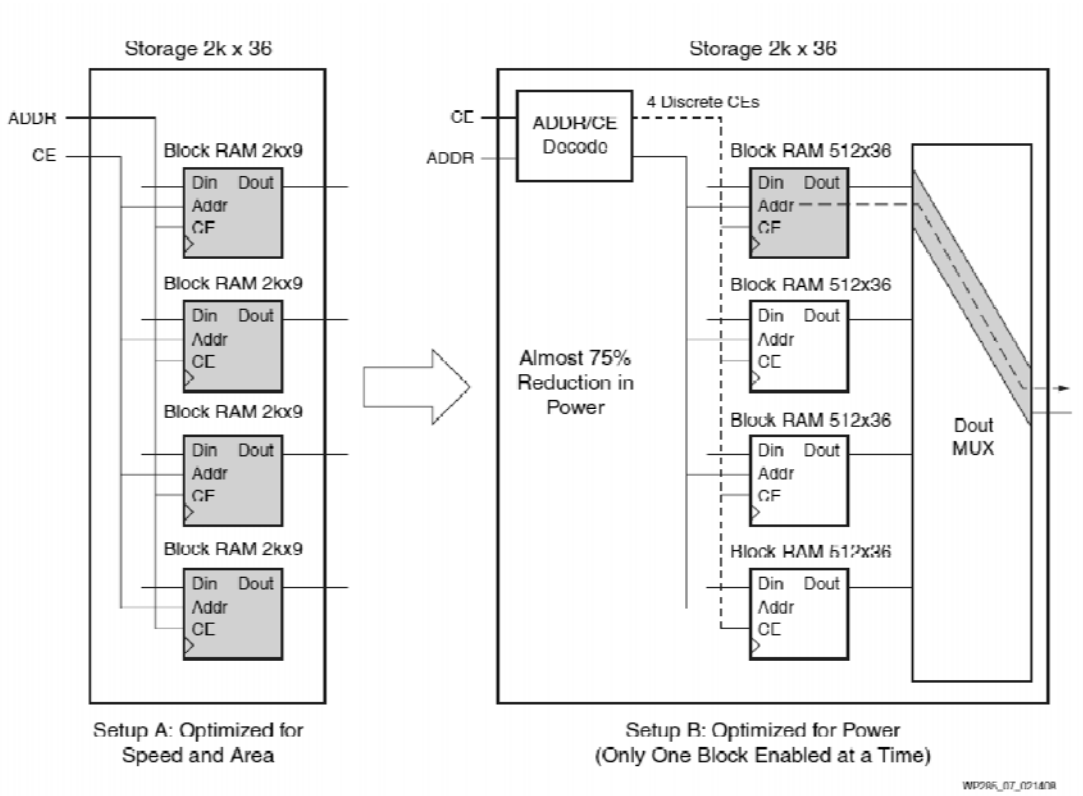
- Block RAMs
  - Enable - ENA, ENB (ENAWREN, ENBRDEN): The enable pin affects the read, write, and set/reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.
  - 1º Detect activation of BlockRam Enables
  - 2º Disable CLK.

Support for Block RAM Low Power Modes

Block RAM can be a major consumer of both static and dynamic power. The Xilinx Synthesis Technology (XST) tool provides block RAM power saving features. The user can use the RAM_STYLE=block_power1/block_power2 attribute to yield significant block RAM power savings for those that choose to infer RAM.

LPD Idea 16: Divide the Memory Map
Xilinx: Reorganizing Block RAM

***Source:** P. Abusaidi, M. Klein, and B. Philofsky, **Virtex-5 FPGA System Power Design Considerations**,* Xilinx Inc. 2008



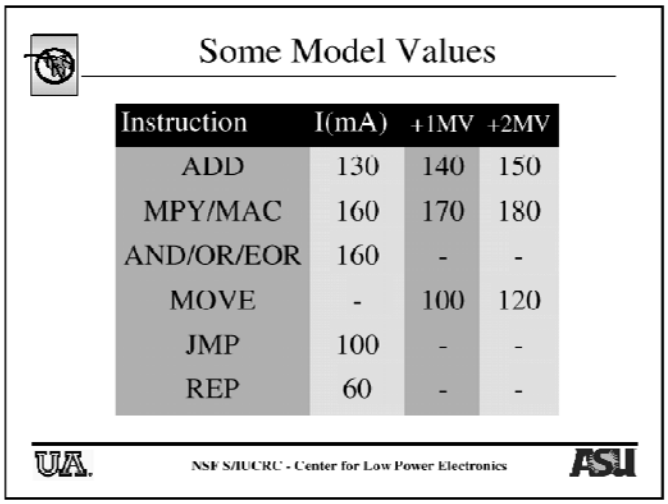
LPD Idea 19: Turn the μP off (power-down)

- Processors can be innactive during long periods.
- Clock power + Static Power still works.
- Idea: *Power-down.*

- Example: Pentium 166 MHz, power pass from 7 W to 1 W in power-down mode.

- **Rule-of-Thumb:** Sometime is better to finish the computation as fast as possible and the turn the processor off. (because the static power always exists and several blocks like the clock tree are always using energy)

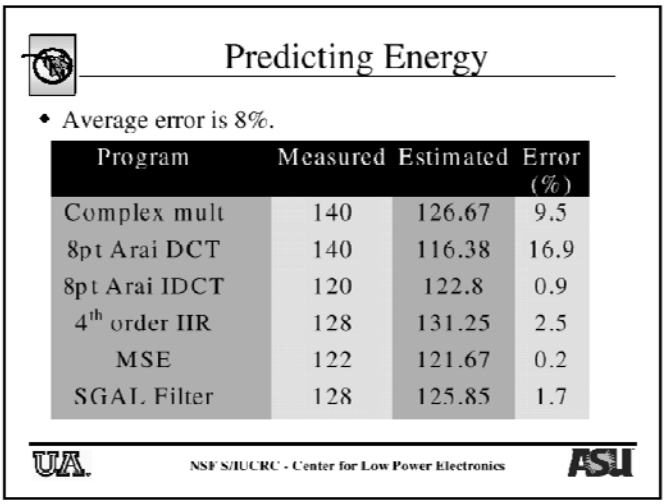
LPD Idea 20: Cold scheduling
Example: Motorola DSP 56309



Some Model Values

Instruction	I(mA)	+1MV	+2MV
ADD	130	140	150
MPY/MAC	160	170	180
AND/OR/EOR	160	-	-
MOVE	-	100	120
JMP	100	-	-
REP	60	-	-

UA NSF S/IUCRC - Center for Low Power Electronics ASU



Predicting Energy

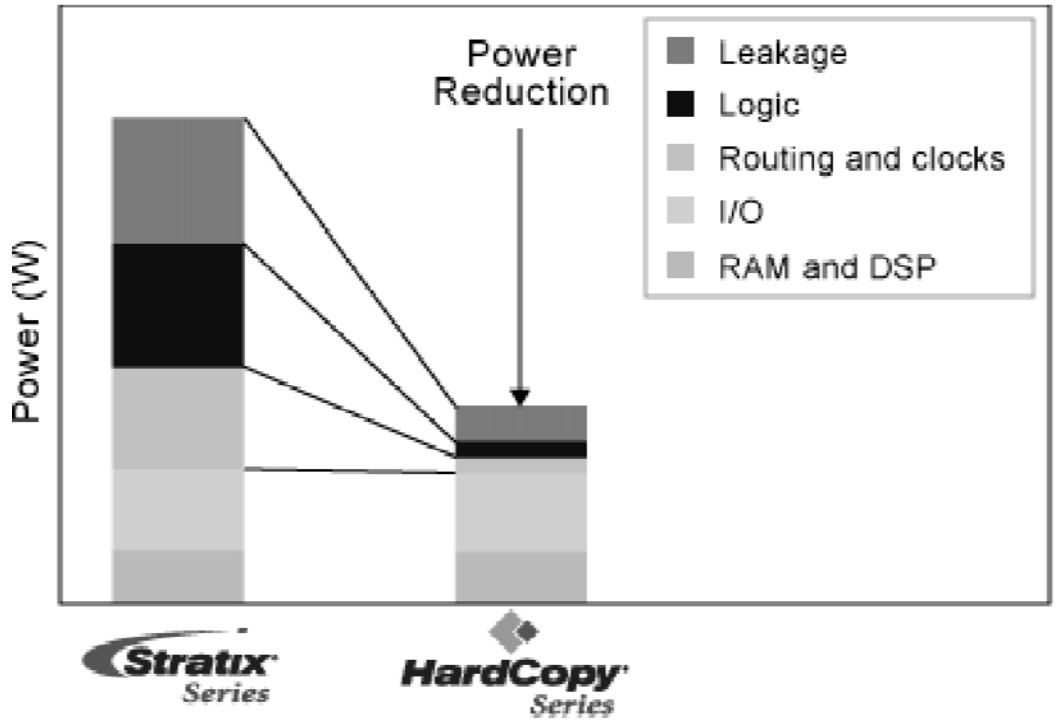
- Average error is 8%.

Program	Measured	Estimated	Error (%)
Complex mult	140	126.67	9.5
8pt Arai DCT	140	116.38	16.9
8pt Arai IDCT	120	122.8	0.9
4th order IIR	128	131.25	2.5
MSE	122	121.67	0.2
SGAL Filter	128	125.85	1.7

UA NSF S/IUCRC - Center for Low Power Electronics ASU

Source*: "Develop efficient DSP compilers",* ***Chaitali Chakrabarti,*** Dept of E.Engineering Arizona State University

LPD Idea 21:
Retargeting from FPGA to structured ASIC

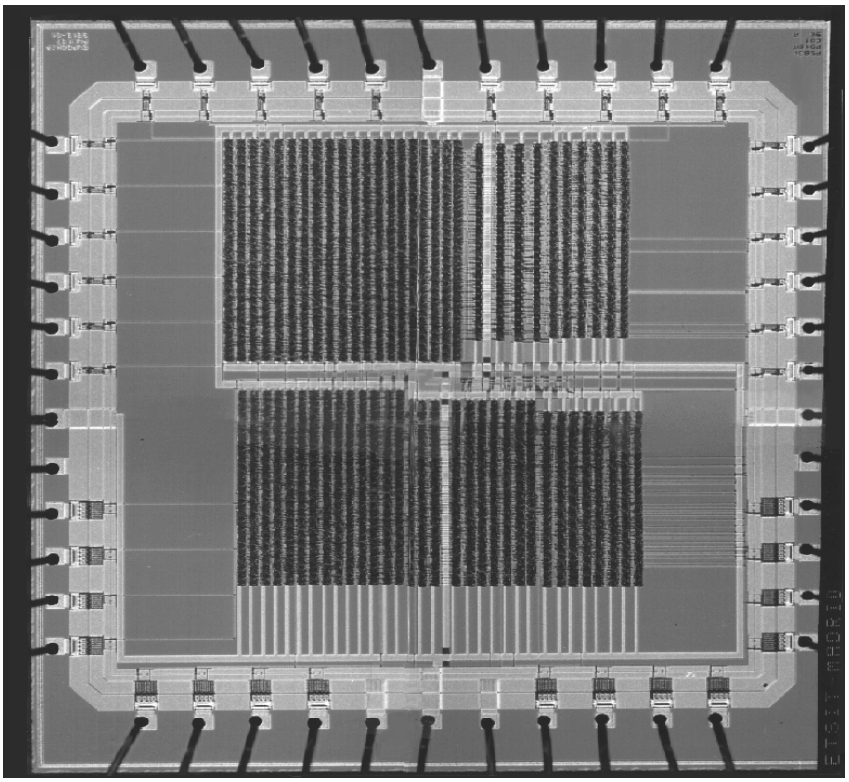


The scale of y-axe?

- **Source**: HardCopy II ASICs: Power Advantage, www.altera.com

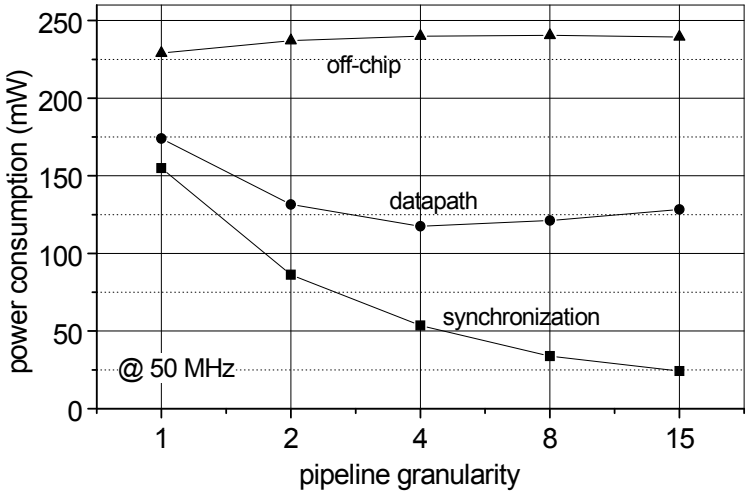
LPD Idea 21: Retargeting from FPGA to structured ASIC

Standard Cells vs. FPGAs: A case-history



LPD Idea 21: Retargeting from FPGA to structured ASIC

Standard Cells vs. FPGAs: A case-history



28-fold lower than FPGA power

Same off-chip power

Fuente: E. Boemo, S. Lopez-Buedo, C. Santos, J. Jauregui and J. Meneses, "Logic Depth and Power Consumption: A Comparative Study between Standard Cells and FPGAs", Proc. XIII DCIS Conference (Design of Circuit and Integrated Systems), Madrid, Universidad Carlos III: November 1998

LPD Idea 22: Power reduction via reconfiguration

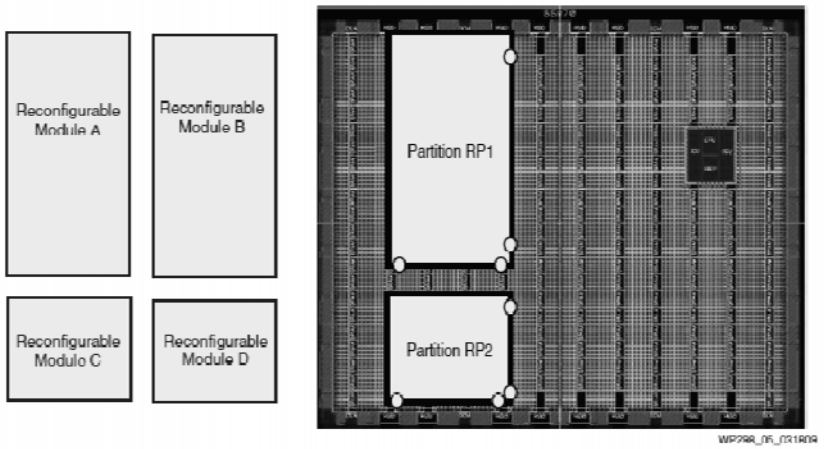


Figure 5: **High-Level Overview of Partial Reconfiguration**

- Parcial reconfiguration allows the designer make use on a smaller FPGA for the same application.
- High engineering cost – lack of tools
- Not always applicable.

Final Remarks

- Low-power design at Scholar Google:

- Entries for low-power design:

  - **1.920.000** (March 2011)
  - **1.120.000** (Feb 2012)

  - Picking-up the main idea in 10 minutes of the 5% smartest works (papers, thesis, app notes, etc) could take 5760 hs

- Entries for low-power design AND FPGA
  - **27.300** (March 2011)
  - **29.600** (Feb 2012)

Final Remarks

- At the university we sometimes invent a problem to solve. Sometimes, this invented problem become the future real problem of the industry.

- 20 years of research in Low-Power Design at Madrid in:

  - http://arantxa.ii.uam.es/~ivan/papers.htm

  - + 100 papers - thousands of experiments.
  - + 8 thesis.
  - Now: LPD, Thermal Aspects, Reliable Design on FPGA.

- Technical Training on FPGA Design Methodology at UAM

  - http://arantxa.ii.uam.es/~euroform/